



TITLE:

# STUDY OF ANALOG COMPUTER TECHNIQUES( Dissertation\_全文 )

AUTHOR(S):

Takahashi, Yoshizo

---

CITATION:

Takahashi, Yoshizo. STUDY OF ANALOG COMPUTER TECHNIQUES. 京都大学, 1964, 工学博士

ISSUE DATE:

1964-06-23

URL:

<https://doi.org/10.14989/doctor.r322>

RIGHT:

# STUDY OF ANALOG COMPUTER TECHNIQUES

July 1963

by

YOSHIZO TAKAHASHI

# STUDY OF ANALOG COMPUTER TECHNIQUES

July, 1963. by Yoshizo Takahashi

	General Intoduction .....	1
Chapt 1	Theory of the Simulation of Network on the Analog Coputer .....	5
1.1	Introduction .....	5
1.2	Signal Flow Graph of the Network .....	6
1.3	Network Simulation .....	7
1.4	Connection Matrix and Mesh Matrix .....	8
1.5	Condition for Network Simulation .....	12
1.6	Finding (Iij) by Sweep-out Method .....	17
1.7	Deriving (Eij) from (Iij) .....	19
1.8	Automatic Programming of Analog Computer by Digital Computer .....	21
Chapt 2	Study of Analog Computer Elements .....	25
2.1	Introduction .....	25
2.2	Patch-Board Design .....	25
2.3	Computer for the Loading Effect Correction of the Potentiometer .....	28
2.4	Evaluation of Time Delay Elements .....	30
2.4.1	Analytical Approach .....	31
2.4.2	Sampled - Delay System .....	33
2.4.3	Magnetic Tape Time Delay Elements .....	36
2.4.4	Concluding Remark .....	38
2.5	Variable Time Delay Element by Stroger Relay .....	39
2.6	Automatic Test Equipment of the Analog Computer .....	40
2.6.1	Introduction .....	40
2.6.2	Automatic Testing of Analog Computer .....	40
2.6.3	Principle of Operation .....	41
2.6.4	Concluding Remark .....	44
Chapt 3	Dynamics of Computing Servomechanisms .....	45
3.1	Introduction .....	45
3.2	Frequency Response .....	46
3.3	Transfer Function of AC Servomechanisms and Compensation Networks .....	51
3.3.1	Introduction .....	51
3.3.2	Transfer Function Calculation .....	52
3.3.3	Example of Calculation .....	56
3.3.4	Concluding Remark .....	58
3.4	Transfer Function of Chopper - Modulated Circuits .....	59
3.4.1	Introduction .....	59
3.4.2	Transient Response of a Simple Chopper - Modulated Circuit .....	60
3.4.3	Non - Resonant Chopper - Modulated Circuits .....	66
3.4.4	Resonant Chopper - Modulated Circuits .....	69
3.4.5	Analyzing the Response of the Chopper - Modulated Circuit by the Analog Computer .....	76
3.4.6	Concluding Remark .....	77
Chapt 4	New Computation Techniques by Analog Computer .....	79
4.1	Calculation of Frequency Response by Analog Computer .....	79
4.2	Fault Current Estimation of Mercury Rectifier Circuit .....	85
4.3	Automatic Programming Applied to Two - Point Boundary Value Problems .....	89
4.3.1	Introduction .....	89

DOC

1964

1

電気系

4.3.2	Eigen Value Problems .....	92
4.3.3	Stability Problem of Automatic Programming .....	93
4.4	Calculation of the Transfer Function of Noisy Processes by the Delay Line Filter .....	99
Chapt 5	Study of the Digitalized Analog Computer .....	107
5.1	Introduction .....	107
5.2	System Design .....	111
5.2.1	General Description of DAC .....	111
5.2.2	Number System .....	112
5.2.3	Integrator .....	113
5.2.4	Coefficient Multiplier .....	117
5.2.5	Servo Element .....	118
5.2.6	Adder .....	118
5.2.7	Multiplier and Divider.....	119
5.2.8	Scaling .....	120
5.3	Logical Design .....	121
5.3.1	Number System .....	121
5.3.2	Gate Circuit .....	121
5.3.3	R Register .....	123
5.3.4	Y Register .....	124
5.3.5	Integrator .....	126
5.3.6	Coefficient Multiplier .....	128
5.3.7	Servo Element .....	129
5.3.8	Adder .....	131
5.4	Model Computer DAC-I .....	132
5.5	Accuracy and Computation Speed of DAC .....	140
5.5.1	Maximum Rate of Change of Variables .....	140
5.5.2	Truncation Error .....	141
5.5.3	Round - Off Error .....	147
5.6	Incremental Calculus .....	155
5.6.1	Polynomial .....	155
5.6.2	Rational Function .....	156
5.6.3	Coordinate Transformation .....	157
5.7	Concluding Remark .....	161
	Conclusion and Acknowledgement .....	162
	References .....	164



## General Introduction

The electronic computer has its source during the World War II and has been developed towards higher accuracy and more flexibility in the operation, to find wider field of application in science and technology. The present prosperity of the analog computer could never been supposed in earlier days, when discussions were mainly on comparison of the analog computer with the digital one as to the accuracy of computation, ease of programming, computation time and so forth. Those discussions originated in the concept that the analog computer is a calculating machine same as a digital computer though the concept was soon found inadequate. With increase of familiarity with computers, the essential difference between these types of computers became obvious. As to the analyst the calculating machine is in open loop condition whereas the analog computer is in closed loop. In other words the calculating machine is used merely to get a result of computation in a way assigned by the analyst. The result of computation by the analog computer, on the other hand, affects the analyst in determining parameters of computation for next runs. Therefore it is preferable to consider the analog computer as a simulator rather than a calculating machine. The simulator is a hardware possessing analytical structure identical with physical system considered. With the simulator one can perform experiments, which are sometimes unexecutable in actual systems and through which one finds hidden properties of the system which were not revealed before the experiment.

Nowadays analog computers are widely used as simulators. Important problems with a simulator are not precision of the individual components but dynamic property of the computing elements and stability of the computing circuit. Also important is the way of representing physical system with the simulator. The research in these problems is necessary both for designing analog computers and analyzing the problems with analog computers.

From 1956 to 1960 the author worked for designing and building a large scale dc analog computer the TOSAC I and II in Tsurumi Research Laboratory of Tokyo - Shibaura Electric Co., Ltd.<sup>1,2)</sup> He also worked for applying those to solving various problems of electrical engineering in the Company.<sup>3)</sup> During the course he investigated dynamic property of computing servomechanism, developed new computing elements, established a general theory of the network simulation with analog computers, and developed new techniques of analysis with analog computers.

Much accuracy was desired in the analog computer calculations with expansion of the application field of simulation technique. The flight simulation and the nuclear reactor simulation now require hundreds of computing elements. Even the highest precision and stability of the computing elements by analog technique are still insufficient for these large scale simulations. So the use of digital technique is almost unavoidable. In this respect attempts to simulate the analog computer on a large scale general purpose digital computer by the program became popular. 4) 5) The author revealed, however, a new way of making the digital computer approach the analog computer. This is the Digitalized Analog Computer, or the DAC in abbreviation. Since 1960 he has been involved in the study of the system of the DAC and worked for designing and building a model computer the DAC - I. During the course of research he established logical structure of computing elements and founded the theory of truncation error as well as round - off error produced with the DAC in solving differential equations. Also done was the study of incremental calculus, which makes the basic operation of the DAC.

The present thesis describes results of the author's research in the analog computer techniques. The thesis is divided into five chapters.

Chapter 1 deals with the programming of the analog computer for solving the response of electrical networks. The block diagram approach for programming analog computer to solve electrical networks, which was developed by the author and has been extensively used in solving actual problems, is not a straightforward method. To complement the block diagram approach the theory of network simulation is investigated. According to this theory, one can readily discriminate whether the given network is representable on the analog computer or not. A method of directly obtaining analog computer circuit of given network is also described.

In Chapter 2 analog computer elements developed by the author are described. Those are the patch - boards, the computer for loading effect correction of potentiometer, the variable time delay element by Stroger relay and the automatic test equipment for the analog computer. These elements were developed from the need in actual analysis of the problems by the analog computer and have proved their extensive usefulness. The time delay element of the analog computer is still unsatisfactory at the present time despite the fact that many types of time delay element have been developed by many people. What is necessary in this circumstance is to discern which type of the time delay elements is more preferable for the particular problem to be treated. In this chapter a quantity

for evaluating the time delay element is proposed and is shown for different types of the time delay element.

Chapter 3 is devoted to the study, from three different aspects, of the dynamic property of computing servomechanisms. The first is the frequency response of the servomechanisms. Usually the desired specification for a computing servomechanism is the maximum frequency of the sinusoidal input signal of certain amplitude to which the servomechanism can follow. The author related the phase plane locus of the mechanical system under sinusoidal motion to the speed - torque curve of the two - phase servomotor and showed the optimum gear ratio necessary to obtain the specification. The second is the study of the way of representing transfer function of ac servomechanisms based on the transient response. A new way of describing the transfer function of ac servomechanisms is obtained and is applied to the design of ac compensating networks and proved its particular usefulness. The third is the study of the transfer function of the chopper - modulated circuits which plays significant part in dynamic property of the servoamplifier. Because the chopper - modulated circuit is a periodically interrupted electrical network, the calculation of the transfer function needs new mathematical procedure. A simultaneous difference equation describing the change of the voltages across the capacitors and the currents in the inductances at a certain time during each interruption period is derived to obtain the transient responses of the periodically interrupted electrical network. In deriving this difference equation, an approximation to replace continuous waveform of the input signal by the staircase function is introduced. The transfer function of the chopper - modulated circuit is obtained by applying the Z transform to this difference equation. The transfer functions of general nonresonant and resonant chopper - modulated circuits are calculated for two typical chopper circuits after they are obtained. An analog computer analysis performed during the course of study has shown a fine example of analog computer techniques using special computer elements.

Chapter 4 is about the new techniques for analog computation developed by the author. Those include a method for obtaining the frequency response from the transient response, calculation of the fault currents of the circuits including mercury rectifiers, automatic programming of analog computer applied to two - point boundary value problems, and a method of calculating transfer functions of noisy processes by using the delay line filter.

Chapter 5 describes the studies of the Digitalized Analog Computer (DAC), i. e. system design, logical design, a model computer DAC - I, accuracy problems of the

computation with the DAC, and the incremental calculus. The DAC is a parallel type digital differential analyzer with the accuracy of one millionth and the computation speed of 0.2 milli - seconds for each step of integration. Although the mathematical operation of the DAC is completely digital, the computer elements of the DAC quite resemble those of the analog computer. The computer elements are the integrator, coefficient multiplier, adder, multiplier etc. They are connected each other on the patch - board <sup>45</sup> with wires just like the analog computer. According to the consideration that the DAC is an analog computer, the solution of the problem is made to be obtained on the pen - recorder. What is required for solving differential equations is not a series of numbers of many digits but the shape or the waveform of the solution. In the DAC the operation in individual computer element is with very high accuracy while the accuracy of the solution displayed is with that of the analog computer. Although the error of the computation with the DAC is small, it has a close relation with the computation speed, which is sometimes important. Generally the error increases as the computation speed is made larger. The computational error of the DAC is divided into the truncation error and the round - off error. In this chapter the mathematical formulation is given both of them by means of the Z transform.

The content of this thesis which is briefly described above is based on the articles of the author, which were published in the Journal of the Institute of Electrical Engineers of Japan, Proceedings of the Joint Conference of Electrical Engineering Societies of Japan, Toshiba Review, Automatic Control, and the Proceedings of the International Analogue Computation Meetings and were supported by many readers.

## Chapter 1

### Theory of the Simulation of Network on the Analog Computer

#### 1.1 Introduction

The basic operation of the differential analyzers such as electronic analog computers, eletromechanical differential analyzers, digital differential analyzers, and differential equation analyzing routines of the general purpose digital computer is the integration. As any ordinary differential equation of single  $\sqrt{\text{Variable}}$  is solved by integration it is solvable by the differential analyzer. But there is a set of problems where integration is not always applicable.

The problem of the electrical network is an example where the circuit equation is a simultaneous differential equation. Should the differential equation of a single variable be derived from this simultaneous differential equation the coefficients of the obtained differential equation are complex functions of the circuit parameters and initial conditions. If, as is usual, we want to find solutions for many combinations of these parameters by the differential analyzer this kind of equations is extremely inconvenient. For solving the network, therefore, the method of the network simulation by which the network is transformed into a block diagram <sup>5)</sup> (or a signal flow graph) to be represented by analog computer elements is preferable to the differential equation method.

The simulation of networks on the ~~anal~~<sup>an</sup>alog computer was first introduced by the author in 1957 when the theory was not completed.<sup>6)</sup> At that time we had to rely upon the trial - and - error method for finding the block diagram which is realizable by the analog computer, that is, containing no differential operation. It is not always possible to construct a unique block diagram containing no differential operation in it or to obtain one.

A solution of this problem was once given by Hirayama.<sup>7)</sup> According to Hirayama the differential operator is eliminated by introducing an amplifier with an infinite gain representing an infinite resistance. From the view point of analog computer circuit this solution is not at all different from that using differentiator. Therefore this cannot be the solution of the present problem.

As the differential analyzer is not equipped with the differentiator differential operation should not appear in the block diagram. Although the analog computer is not unable to make differentiators, they cause noise amplification and instability

in the analog computer circuit and their use should be avoided by any means. As the result finding the block diagram of the given electrical network containing no differential operation is required

The author has developed a general theory of the network simulation to find under what condition is or is not the simulation of the network by the analog computer possible. He has also shown a straightforward method of building the analog computer circuit simulating the network once its existence is proved. The followings are the details of the theory and the examples.

## 1.2 Signal Flow Graph of the Network

Although the network we are going to discuss is limited to the electrical network the following theory also applies to mechanical, thermal and any other networks. In those non - electrical networks the words inductance, capacitance and resistance may be replaced by proper terms.

As the first step towards the theory of the network simulation the method of transforming the network into the block diagram is studied. The network of Fig.

1.1 (a) is one for which the simulation is possible. Denoting the currents and the voltages of the network as shown in the circuit diagram the block diagram of the network is constructed as shown in Fig. 1.1 (a).

The network of Fig. 1.2 (a) is an example for which the simulation is not possible. By any means the block diagram of this network becomes one similar to Fig. 1.2 (b) which unavoidably contains differential operation. Thus the possibility of the network simulation depends on the configuration of the network and it is often laborious to make out the possibility by trying to build many

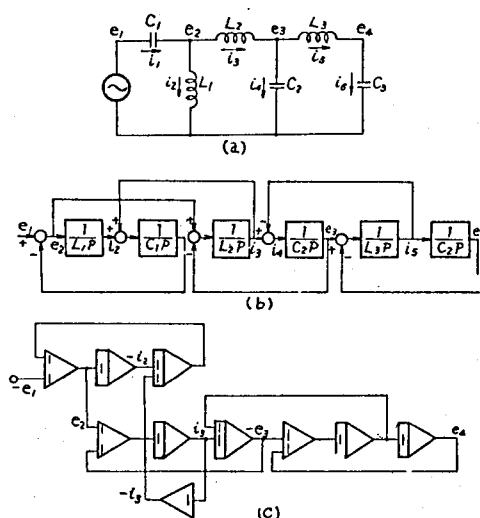


Fig. 1.1 Block diagram  
Approach of network (b) block diagram (c) analog computer circuit.

block diagrams for the given network.

There are more than one block diagrams

for one network. Even when an obtained

block diagram cannot be simulated there might

be other block diagrams which are simulatable.

It is therefore quite important to have the

criterion of the possibility of the network

simulation. 8) 9) 10)

### 1.3 Network Simulation

Consider an electrical network having no isolated part and consisting of the following elements. ( In case mutual inductances exist in the original network they should be removed by equivalent transformation of the network. The negative self-inductances are permitted in the following discussion.)

C	capacitances	$C_1, C_2, \dots, C_c$
L	inductances	$L_1, L_2, \dots, L_c$
R (=R <sub>1</sub> +R <sub>2</sub> )	resistances	$R_1, R_2, \dots, R_{R1}$ $R'_1, R'_2, \dots, R'_{R2}$
E	voltage sources	$E_1, E_2, \dots, E_e$
S	current sources	$S_1, S_2, \dots, S_s$

Denoting the voltage - drops and branch currents in these elements  $e$  and  $i$  respectively, the relations between them will be represented in the signal flow graphs of Fig. 1.3. Notice that the differential relation is excluded. For the resistance the direction of the signal flow is unrestricted. The direction of voltages and the currents in the voltage source and the current source are defined as shown in Fig 1.4.

Now if the simulation of this network is possible the overall signal flow graph of the simulation circuit will be shown as Fig. 1.5.

The I - and E matrix circuits

represent the first and the

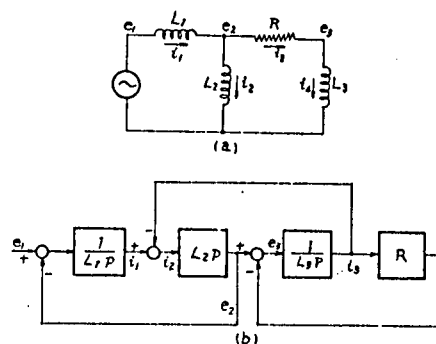


Fig. 1.2 Example of a network for which the simulation is impossible; (a) network (b) block diagram.

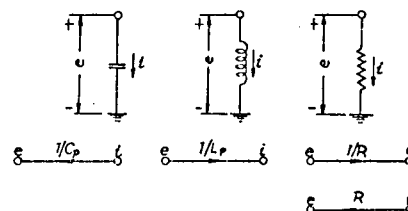


Fig. 1.3 Signal flow graph representation of the circuit elements. The differentiations are excluded.

second Kirchhoff's laws respectively; that is, these matrix circuits are defined by the configuration of the original network. Although the voltage drops of the current sources and the branch currents of the voltage sources are meaningless they are included in the signal flow graph for the convenience of the discussion.

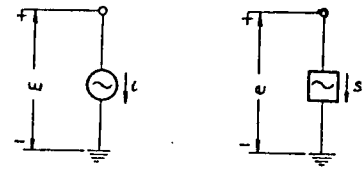


Fig. 1.4 Signal flow graph representation of the voltage source and the current source

It should also be noted that the resistances are divided into two groups  $R$  and  $R'$  in building signal flow graph.

The principle of classifying the resistances will be explained in the following sections. As shown in Fig. 1.3 resistances of  $R$  group are considered

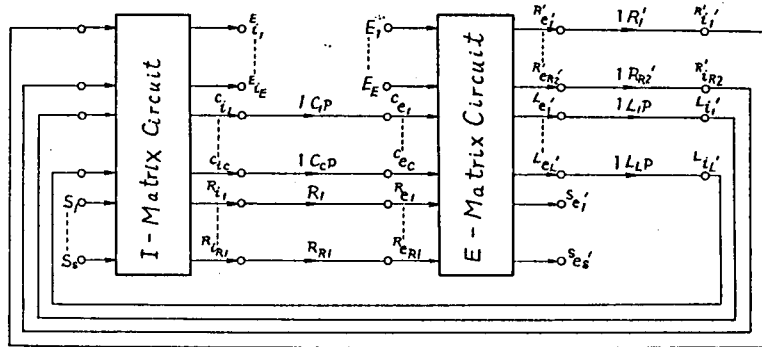


Fig. 1.5 Signal flow graph of a general electrical network.

elements converting currents into voltages as

capacitances do and those of  $R$  group are considered elements converting voltages into currents as inductances do, From the above discussion it is concluded that.

"The network simulation is the construction of  $I$  - and  $E$  - matrix circuits for a given network."

#### 1.4 Connection Matrix and Mesh Matrix

The  $I$  - matrix circuit defines Kirchhoff's first law. The input signals of the  $I$  - matrix circuit are the currents in resistances of  $R'$  group  $R_{i_1}', R_{i_2}', \dots, R_{i_{R2}}'$ , the currents in the inductances  $L_{i_1}', L_{i_2}', \dots, L_{i_L}'$ , and the currents of the current sources  $S_1, S_2, \dots, S_s$ . Those are written in this order as  $i_1', i_2', \dots, i_M'$ . Output signals of the  $I$  - matrix circuit are the currents in the voltage sources  $E_{i_1}, E_{i_2}, \dots, E_{i_E}$ , the currents in the capacitances  $C_{i_1}, \dots, C_{i_C}$ , and the currents in the resistances of  $R$  group  $R_{i_1}, R_{i_2}, \dots, R_{i_{R1}}$ . Those are written in this order as  $i_1, i_2, \dots, i_N$ .

As the number of the modal equations due to the Kirchhoff's first law is that of



the independent nodes of the network N, there are N output signals for the I - matrix circuit. (There are N + 1 nodes for an unisolated network in total.) For the network which has no isolated part the next relationship concerning the number of branches B, the number of independent meshes M and the number of independent nodes N always holds. <sup>11)</sup>

$$M + N = B \quad (1.1)$$

The number of input signals to the I - matrix circuit is, therefore, M. The equation describing the relation between input and output of the I - matrix circuit is then

$$\begin{pmatrix} i_1 \\ i_2 \\ \cdot \\ \cdot \\ \cdot \\ \cdot \\ i_N \end{pmatrix} = (I_{ij}) \begin{pmatrix} i_1' \\ i_2' \\ \cdot \\ \cdot \\ \cdot \\ \cdot \\ i_M' \end{pmatrix} \quad (1.2)$$

(I<sub>ij</sub>) is a matrix of N rows and M columns and the elements are either 0, 1 or -1. As is obvious from the definition of  $i_1, i_2, \dots, i_N$  and  $i_1', i_2', \dots, i_M'$  the following relations exist among the numbers of the elements of the network.

$$\left. \begin{aligned} E + C + R_1 &= N \\ R_2 + L + S &= M \end{aligned} \right\} \quad (1.3)$$

The E - matrix circuit defines the relation among the voltage - drops of the branches of the network determined by the Kirchhoff's second law. The input signals to this matrix circuit <sup>(12)</sup> is then

$$\begin{pmatrix} e_1' \\ e_2' \\ \cdot \\ \cdot \\ \cdot \\ \cdot \\ e_M' \end{pmatrix} = (E_{ij}) \begin{pmatrix} e_1 \\ e_2 \\ \cdot \\ \cdot \\ \cdot \\ \cdot \\ e_N \end{pmatrix} \quad (1.4)$$

(E<sub>ij</sub>) is a matrix of M rows and N columns and the element are again either 0, 1 or - 1.

Now the nodal equations of the network are written in a single equation as

$$(D_{ij}) \begin{pmatrix} i_1 \\ i_2 \\ \vdots \\ i_B \end{pmatrix} = 0, \quad (1.5)$$

where  $i_1, i_2, \dots, i_B$  are the branch currents and  $(D_{ij})$  is the connection matrix of which elements take value of either 0, 1 or -1. <sup>12)</sup>

$$(D_{ij}) = \begin{pmatrix} D_{11} & D_{12} & \dots & D_{1B} \\ D_{21} & D_{22} & \dots & D_{2B} \\ \dots & \dots & \dots & \dots \\ D_{N1} & D_{N2} & \dots & D_{NB} \end{pmatrix} \quad (1.6)$$

The element of the connection matrix,  $D_{ij}$ , is 1 when  $j$ th branch current flows into the  $i$ th node, -1 when it flows out of that node and is zero when the  $j$ th branch is not connected to the  $i$ th node.

To explain the connection matrix by an example the electrical network of Fig. 1.6 is shown. Assigning numbers to all branches and all independent nodes as shown in the figure the following connection matrix is obtainable.

$$(D_{ij}) = \begin{pmatrix} -1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & -1 & -1 & -1 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & -1 & 0 & 0 & 0 & 1 & -1 \end{pmatrix} \quad (1.7)$$

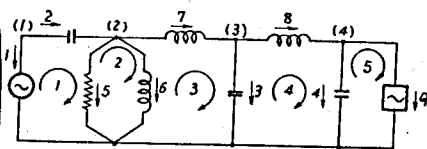


Fig. 1.6 Electrical network for which number nodes is denoted (1), (2),... number of branches by 1, 2, ..., and number of meshes by 1, 2, ....

The relation among the branch voltages of the network determined by the Kirchhoff's second law is represented by the following matrix equation.

$$(R_{ij}) \begin{pmatrix} e_1 \\ e_2 \\ \vdots \\ e_B \end{pmatrix} = 0 \quad (1.8)$$

where  $e_1, e_2, \dots, e_B$  are the voltage drops of the branches and  $(R_{ij})$  is the mesh matrix which is

$$(R_{ij}) = \begin{pmatrix} R_{11} & R_{12} & \dots & R_{1B} \\ R_{21} & R_{22} & \dots & R_{2B} \\ \dots & \dots & \dots & \dots \\ R_{M1} & R_{M2} & \dots & R_{MB} \end{pmatrix} \quad (1.9)$$

$R_{ij}$  is 1 when  $j$ th branch is connected clockwise in the  $i$ th mesh, -1 when it is connected counterclockwise in this mesh, and is zero when it is not connected in the  $i$ th mesh. As an example the mesh matrix of the network of Fig. 1.6 is given below,

$$(R_{ij}) = \begin{pmatrix} -1 & 1 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & -1 & 1 & 0 & 0 \\ 0 & 0 & -1 & 1 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & -1 & 0 & 0 & 0 & 0 & 1 \end{pmatrix} \quad (1.10)$$

The branch currents  $i_1, i_2, \dots, i_B$  are related to the mesh currents ~~currents~~  $I_1, I_2, \dots, I_M$  by the mesh matrix as

$$\begin{pmatrix} i_1 \\ i_2 \\ \vdots \\ i_B \end{pmatrix} = (R_{ij})^t \begin{pmatrix} I_1 \\ I_2 \\ \vdots \\ I_M \end{pmatrix} \quad (1.11)$$

because a branch current  $i_i$  is the algebraic sum of the mesh currents; that is

$$i_i = \sum_{j=1}^M a_{ij} I_j$$

$a_{ij}$  is 1 when  $I_j$  flows <sup>↑</sup> along the  $i$ th branch, -1 when it flows <sup>↓</sup> against this branch, and zero when  $I_j$  does not flow through this branch. Therefore

$$D_{ij} = D_{ji} \quad (1.12)$$

From eq. (1.11) and eq. (1.5) we obtain

$$(D_{ij}) \cdot (R_{ij})^t = 0$$

This relation connecting the mesh matrix and the connection matrix is useful in deriving the relation between the  $I$ -matrix circuit and the  $E$ -matrix circuit as will be shown later.

## 1.5 Condition for the Network Simulation

As was pointed out already by the example of the network of Fig. 1.2 the simulation of the network is not always possible. The condition that the network simulation is possible is now investigated. As stated in Section 1.3 the network simulation is to define I - and E - matrix circuits. As will be shown in later section the E - matrix circuit is uniquely determined by the I - matrix circuit.<sup>13)</sup> Therefore the condition for the possibility of the network simulation is the existence of the I - matrix circuit. The problem is whether eq. (1.2) can be derived from the nodal equation eq. (1.5) or not.

The nodal equation eq. (1.5) is rewritten in the next form recollecting eq. (1.1) and the way of dividing branch currents into groups of  $i$  and those of  $i'$

$$\begin{pmatrix} D_{11} & D_{12} & \dots & D_{1N} & D'_{11} & D'_{12} & \dots & D'_{1M} \\ D_{21} & D_{22} & \dots & D_{2N} & D'_{21} & D'_{22} & \dots & D'_{2M} \\ \cdot & \cdot & & \cdot & \cdot & \cdot & & \cdot \\ \cdot & \cdot & & \cdot & \cdot & \cdot & & \cdot \\ \cdot & \cdot & & \cdot & \cdot & \cdot & & \cdot \\ D_{N1} & D_{N2} & \dots & D_{NN} & D'_{N1} & D'_{N2} & \dots & D'_{NM} \end{pmatrix} \begin{pmatrix} i_1 \\ i_2 \\ \cdot \\ \cdot \\ i_N \\ i'_1 \\ i'_2 \\ \cdot \\ \cdot \\ i'_M \end{pmatrix} = 0 \quad (1.13)$$

The matrix  $(D_{ij})$  is here divided into two minor matrices  $D_1$  and  $D_2$  which are

$$D_1 = \begin{pmatrix} D_{11} & D_{12} & \dots & D_{1N} \\ D_{21} & D_{22} & \dots & D_{2N} \\ \dots & \dots & \dots & \dots \\ D_{N1} & D_{N2} & \dots & D_{NN} \end{pmatrix} \quad (1.14)$$

$$D_2 = \begin{pmatrix} D'_{11} & D'_{12} & \dots & D'_{1M} \\ D'_{21} & D'_{22} & \dots & D'_{2M} \\ \dots & \dots & \dots & \dots \\ D'_{N1} & D'_{N2} & \dots & D'_{NM} \end{pmatrix} \quad (1.15)$$

Eq. (1.13) is then written

$$D_1 \cdot \begin{pmatrix} i_1 \\ i_2 \\ \vdots \\ i_N \end{pmatrix} + D_2 \cdot \begin{pmatrix} i_1' \\ i_2' \\ \vdots \\ i_M' \end{pmatrix} = 0 \quad (1.16)$$

The necessary and the sufficient condition that this equation is solvable for  $i_1, i_2, \dots, i_N$  is that  $D_1$  is regular, or

$$\text{Det } D_1 \neq 0 \quad (1.17)$$

when this condition is satisfied, multiplying  $D_1^{-1}$  from the left and rearranging give eq.(1.2). (1.17) is then written

$$(I_{ij}) = -D_1^{-1} \cdot D_2 \quad (1.18)$$

Now we attained a new statement concerning the condition of the network simulation; the necessary and the sufficient condition that the network simulation is possible is that a regular matrix  $D_1$  is obtainable from the connection matrix of the network  $(D_{ij})$ . The next problem to be studied is the connection of this condition to the configuration of the network.

The matrix  $D_1$  is a square matrix whose columns are those of the connection matrix representing the branches of voltage sources, capacitances and resistances of R group. It is therefore necessary that there are  $R_1$  resistances satisfying eq.(1.3). In other words it is necessary that the number of independent nodes is not less than the sum of the numbers of voltage sources and capacitances of the network and not larger than the sum of the numbers of voltage sources, capacitances and resistances. The voltage sources, the capacitances and the resistances are named eligible branches. This is written in the following theorem.

( Theorem 1.1 ) To be possible to simulate a network on the analog computer it is necessary that the following inequality is satisfied by the elements and the configuration of the network.

$$0 \leq N - C - E \leq R \quad (1.19)$$

As this is a necessary condition the simulation is obviously not always possible even when ineq.(1.19) may be satisfied. This theorem is, however, useful for identifying networks for which the simulation is impossible. The network of Fig. 1.1 for example, satisfies ineq.(1.19) because

$$N = 4, E = 1, C = 3, R = 0$$

$$N - C - E = 0$$

while that of Fig. 1.2 does not, because

$$N = 3, E = 1, C = 0, R = 1$$

$$N - C - E = 2 > R$$

Thus we can prove that the latter network is unable to simulate as was inferred in Section 1.2.

When ineq.(1.19) is satisfied by a network at least the matrix  $D_1$  exists for this network although the regularity is yet to be tested. Once a regular matrix  $D_1$  is found by taking suitable  $R_1$  columns out of  $R$  columns of the connection matrix related to the resistances of the network, the simulation of this network is possible. After investigating the condition that  $D_1$  is regular the following lemmas were obtained.

( Lemma 1.1 ) If any branches which are members of  $N$  branches composing columns of the matrix  $D_1$  make a mesh, then  $D_1$  is not regular.

( Proof ) Assume that the first  $n$  of  $N$  branches make a mesh as Fig. 1.7.  $D_1$  is then written as

$$D_1 = \begin{pmatrix} -1 & 0 & \dots & 0 & 1 & x & \dots & x \\ 1 & -1 & \dots & 0 & 0 & x & \dots & x \\ \dots & \dots & \dots & \dots & \dots & \dots & \dots & \dots \\ 0 & 0 & \dots & 1 & -1 & x & \dots & x \\ 0 & 0 & \dots & 0 & 0 & x & \dots & x \\ \dots & \dots & \dots & \dots & \dots & \dots & \dots & \dots \\ 0 & 0 & \dots & 0 & 0 & x & \dots & x \end{pmatrix} \quad (1.20)$$

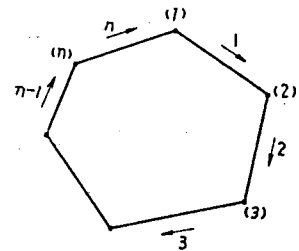


Fig. 1.7 A Mesh for which  $\det. D_1$  is always zero

As the sum of the first  $n$  columns results a zero vector  $\det D_1$  is zero.

( Lemma 1.2 ) If  $N$  branches composing columns of the matrix  $D_1$  make a tree <sup>14)</sup>, then  $D_1$  is regular.

( Proof ) Assume that these  $N$  branches make a tree such as shown in Fig. 1.8. The branches which are the ends of the tree are numbered 1.2 ...,  $n$ . The matrix  $D_1$  is then written

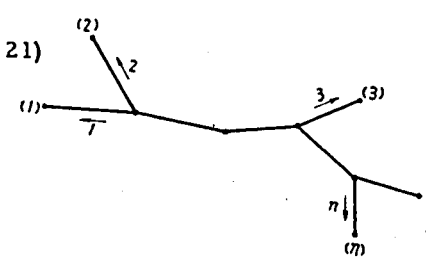
$$D_1 = \begin{pmatrix} \overbrace{1 \ 0 \ \dots \ 0}^n & \overbrace{0 \ \dots \ 0}^{N-n} \\ 0 \ 1 \ \dots \ 0 & 0 \ \dots \ 0 \\ \dots & \dots \\ 0 \ 0 \ \dots \ 1 & 0 \ \dots \ 0 \\ x \ x \ \dots \ x & \boxed{D'_1} \\ \dots & \dots \\ x \ x \ \dots \ x & \dots \end{pmatrix} \quad (1.21)$$


Fig. 1.8 Tree for which  $D_1$  is always regular.

The  $n$ th principal matrix being unitary whereas remaining nonprincipal minor matrices are zero matrices.

Therefore

$$\det D_1 = \det D'_1 \quad (1.22)$$

$D'_1$  is the connection matrix of the tree which is obtained by removing  $n$  end branches of the original tree. By continuing the process of removing end branches from the tree a star is finally obtained. The star is a set of branches connected at a node. If this node is the unimportant node of the original network the connection matrix of this star takes the next form

$$D'_1 = \begin{pmatrix} \pm 1 & 0 & \dots & 0 \\ 0 & \pm 1 & \dots & 0 \\ \dots & \dots & \dots & \dots \\ 0 & 0 & \dots & \pm 1 \end{pmatrix}$$

and if an end of this star is the unimportant node of the original network the connection matrix takes the next form

$$D'_1 = \begin{pmatrix} \pm 1 & 0 & \dots & 0 \\ 0 & \pm 1 & \dots & 0 \\ \dots & \dots & \dots & \dots \\ \pm 1 & \pm 1 & \dots & \pm 1 \end{pmatrix}$$

In either case  $\det D'_1$  is  $\pm 1$ . Consequently

$$\det D_1 = \pm 1 \neq 0 \quad (1.23)$$

Thus Lemma 1.2 is proved.

The inverse of this lemma is also true as is proved by Lemma 1.1.

Obviously the number of nodes of the tree made from  $N$  branches is  $N + 1$  which is same to the number of nodes of the original network. Therefore that the  $N$  branches make a tree is equivalent to that all nodes of the network are connected

together by these  $N$  branches, which are the voltage sources, the capacitances and the resistances. This is written in the following theorem.

( Theorem 1.2 )                      The necessary and the sufficient condition that the simulation of a network by the analog computer is possible is that all nodes of the network are connected together by all of the branches composing  $N$  columns of the matrix  $D_1$ .

In the network of Fig. 1.11, for example, four nodes (1), (2), (3), (4) and (5) are not connected by the branches of 1, 2, 3 and 4. This network is therefore unable to simulate. In the network of Fig. 1.10 nodes (1), (2), (3) and (4) are connected either by the branches of 1, 2 and 3, by those of 1, 2 and 4 or by those of 1, 3 and 4.  $D_1$  is regular for this network. In special networks where an inductance is connected in series to a current source this junction is isolated from other nodes by eligible branches (voltage source, capacitance or resistance) so that  $D_1$  is not regular irrespective of the remaining part of the network. Similarly when the network contains a capacitance connected parallel with a voltage source  $D_1$  is not regular as this makes a mesh in eligible branches ( Lemma 1.1 )

Summarizing theorem 1.1 and theorem 1.2 the condition that the simulation of a network by the analog computer is possible is stated as follows.

"The necessary and the sufficient condition that the simulation of a network by the analog computer is possible is that the sum of the numbers of the voltage sources and the capacitances of the network never exceeds the number of independent nodes and all nodes of the network are connected together by all of the voltage sources, all of the capacitances and the  $(N - E - C)$  resistances."

EX. 1.1                      For the network of Fig. 1.9 following relation exists.

$$N - C - E = 4 - 2 - 1 - R$$

The eligible branches are 1, 2, 3 and 4 which connects five nodes together, so that the simulation is possible. Actually  $D_1$  is regular as

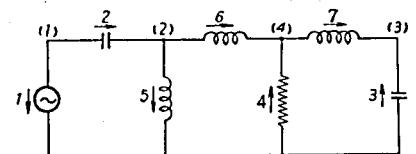


Fig. 1.9 Electrical network. The simulation is possible

$$\det D_1 = \begin{vmatrix} -1 & -1 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{vmatrix} = -1 \neq 0$$



EX. 1.2 For the network of Fig. 1.10  
following relation exists.

$$N - C - E = 2 < R$$

This satisfies ineq.(1.19) of Theorem 1.1.

Any two of three resistances 2, 3 and 4 connect four nodes together with branch 1. As the matter of fact three regular  $D_1$  matrices are obtainable from the connection matrix of this network which is

$$(D_{ij}) = \begin{pmatrix} -1 & 0 & 0 & 0 & -1 & 0 & 0 \\ 0 & 1 & -1 & 0 & 1 & -1 & 0 \\ 0 & 0 & 1 & 1 & 0 & 0 & 1 \end{pmatrix}$$

They are

$$D_1 = \begin{pmatrix} -1 & 0 & 0 \\ 0 & 1 & -1 \\ 0 & 0 & 1 \end{pmatrix} \begin{pmatrix} -1 & 0 & 0 \\ 0 & -1 & 0 \\ 0 & 1 & 1 \end{pmatrix} \text{ and } \begin{pmatrix} -1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{pmatrix}$$

In this case the simulation circuit is not uniquely determined.

EX. 1.3 For the network of Fig. 1.11  
following relation exist.

$$N - C - E = 1 = R$$

This satisfies ineq.(1.19). The five nodes are not connected together by eligible branches 1, 2, 3 and 4. The simulation of this network is not possible.

In fact  $D_1$  is not regular.

$$\det D_1 = \begin{vmatrix} -1 & 0 & 0 & 0 \\ 0 & -1 & -1 & 0 \\ 0 & 1 & 0 & -1 \\ 0 & 0 & 1 & 1 \end{vmatrix} = 0$$

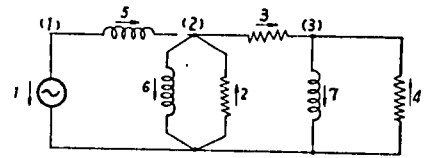


Fig. 1.10 Electrical network.  
The simulation is possible but not uniquely determined.

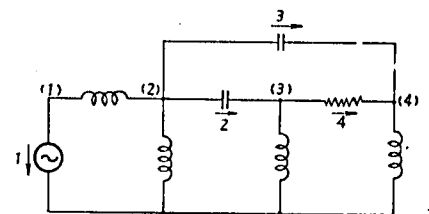


Fig. 1.11 Electrical network  
The simulation is impossible as branches 2, 3 and 4 compose a mesh.

## 1.6 Finding $(I_{ij})$ by Sweep - Out Method

Once the condition for the simulation of a network is satisfied the I - and E - matrix circuits exist for this network. The method of obtaining these two matrix circuits is now considered. The problem is how  $(I_{ij})$  and  $(E_{ij})$  are to be derived from  $(D_{ij})$ .

( Iij ) is already obtained in eq.(1.18). It is preferable, however, to use the sweep-out method for obtaining ( Iij ). As was done in Section 1.5 the connection matrix is separated into two minor matrices  $D_1$  and  $D_2$ . As every column of the connection matrix does not contain more than one 1 and -1 respectively besides 0, adding a row having -1 in the first column to one having 1 in the same column results only one -1 in the first column. The row having this -1 in the first column is now transferred to the first row. In case the first column does not contain 1 and -1 together but either one of them, we merely bring the row having it to the first row after changing the sign of this row if it is 1.

We proceed next to the second column and add a row having 1 in this column at the rows other than the first to those having -1 in the same column. By repeating the similar procedure to the N th column a matrix of which first N columns make a diagonal matrix of -1 is obtained. It is like

$$\begin{pmatrix} -1 & 0 & 0 & \dots & 0 & x_{11} & x_{12} & \dots & x_{1M} \\ 0 & -1 & 0 & \dots & 0 & x_{21} & x_{22} & \dots & x_{2M} \\ 0 & 0 & -1 & \dots & 0 & x_{31} & x_{32} & \dots & x_{3M} \\ \dots & \dots & \dots & \dots & \dots & \dots & \dots & \dots & \dots \\ 0 & 0 & 0 & \dots & -1 & x_{N1} & x_{N2} & \dots & x_{NM} \end{pmatrix} \quad (1.24)$$

The remaining M columns make ( Iij ).

$$(Iij) = \begin{pmatrix} x_{11} & x_{12} & \dots & x_{1M} \\ x_{21} & x_{22} & \dots & x_{2M} \\ \dots & \dots & \dots & \dots \\ x_{N1} & x_{N2} & \dots & x_{NM} \end{pmatrix} \quad (1.25)$$

As the currents in the voltage sources, which appear in the output of the I - matrix circuit, are unnecessary in the actual simulation this first E rows of this ( Iij ) should be ignored in building simulation circuit.

EX. 1.4            The network of Fig. 1.12 satisfies the condition for the network simulation as

$$N - C - E = 6 - 2 - 1 = 3 < R$$

and all nodes are connected by the eligible branches 1, 2, 3, 4, 5 and 6.

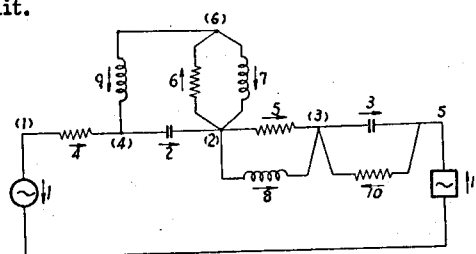


Fig. 1.12 Electrical network. The simulation is possible.

The connection matrix of this network is given by

$$(D_{ij}) = \begin{pmatrix} -1 & 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & -1 & -1 & 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 1 & 0 & 0 & 1 & 0 & 1 & 0 \\ 0 & -1 & 0 & 1 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 1 \\ 0 & 0 & 0 & 0 & 0 & 1 & -1 & 0 & -1 & 0 & 0 \end{pmatrix}$$

After sweeping - out from the first to the sixth column the next matrix results.

$$\begin{pmatrix} -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & -1 \\ 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & -1 \\ 0 & 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & -1 \\ 0 & 0 & 0 & 0 & -1 & 0 & 0 & -1 & 0 & 0 & -1 \\ 0 & 0 & 0 & 0 & 0 & -1 & 1 & 0 & 1 & 0 & 0 \end{pmatrix}$$

(I<sub>ij</sub>) is therefore

$$(I_{ij}) = \begin{pmatrix} 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 & -1 \\ 0 & 0 & 0 & 1 & -1 \\ 0 & 0 & 0 & 0 & -1 \\ 0 & -1 & 0 & 0 & -1 \\ 1 & 0 & 1 & 0 & 0 \end{pmatrix}$$

The input and output relation of I - matrix circuit is

$$\begin{pmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \\ i_5 \\ i_6 \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 & -1 \\ 0 & 0 & 0 & 1 & -1 \\ 0 & 0 & 0 & 0 & -1 \\ 0 & -1 & 0 & 0 & -1 \\ 1 & 0 & 1 & 0 & 0 \end{pmatrix} \begin{pmatrix} i_7 \\ i_8 \\ i_9 \\ i_{10} \\ i_{11} \end{pmatrix} \quad (1.26)$$

#### 1.7 Deriving (E<sub>ij</sub>) from (I<sub>ij</sub>)

To complete the simulation circuit of a network the matrix (E<sub>ij</sub>) should be obtained. This matrix is obtainable by sweeping out the mesh matrix (R<sub>ij</sub>). But the mesh matrix is less convenient to handle than the connection matrix.

As pointed out already in Section 1.4 (Eij) is derivable from (Iij). Now we study how this is done. The mesh equation eq.(1.8) is rewritten as

$$\begin{pmatrix} R_{11} & R_{12} & \dots & R_{1N} & R_{11}' & R_{12}' & \dots & R_{1M}' \\ R_{21} & R_{22} & \dots & R_{2N} & R_{21}' & R_{22}' & \dots & R_{2M}' \\ \dots & \dots & \dots & \dots & \dots & \dots & \dots & \dots \\ R_{M1} & R_{M2} & \dots & R_{MN} & R_{M1}' & R_{M2}' & \dots & R_{MM}' \end{pmatrix} \begin{pmatrix} e_1 \\ \cdot \\ \cdot \\ e_N \\ e_1' \\ e_2' \\ \cdot \\ \cdot \\ e_M \end{pmatrix} = 0 \quad (1.27)$$

Denoting the minor matrix composed of the first N columns of (Rij) by R<sub>1</sub> and the remaining minor matrix of M x M elements by R<sub>2</sub> eq.(1.27) is written

$$R_1 \cdot \begin{pmatrix} e_1 \\ e_2 \\ \cdot \\ \cdot \\ e_N \end{pmatrix} + R_2 \cdot \begin{pmatrix} e_1' \\ e_2' \\ \cdot \\ \cdot \\ e_M' \end{pmatrix} = 0 \quad (1.28)$$

from which the next equation is obtained if the regularity of R<sub>2</sub> is assumed.

$$\begin{pmatrix} e_1' \\ e_2' \\ \cdot \\ \cdot \\ e_M' \end{pmatrix} = -R_2^{-1} \cdot R_1 \cdot \begin{pmatrix} e_1 \\ e_2 \\ \cdot \\ \cdot \\ e_N \end{pmatrix} \quad (1.29)$$

As this equation is identical to eq.(1.4), (Eij) is obtained as

$$(Eij) = -R_2^{-1} \cdot R_1 \quad (1.30)$$

Now the previously obtained eq.(1.12) connecting (Dij) to (Rij) is rewritten in terms of partial matrices D<sub>1</sub>, D<sub>2</sub>, R<sub>1</sub> and R<sub>2</sub> as

$$D_1 \cdot R_1^t + D_2 \cdot R_2^t = 0 \quad (1.31)$$

Multiplying D<sub>1</sub><sup>-1</sup> from the left and (R<sub>2</sub><sup>-1</sup>)<sup>t</sup> from the right gives

$$R_1^t \cdot (R_2^{-1})^t + D_1^{-1} \cdot D_2 = 0 \quad (1.32)$$

The first term of the left hand side of the equality is  $-(E_{ij})$  and the second term is  $(I_{ij})^t$  according to eq.(1.18). Therefore

$$(E_{ij}) = -(I_{ij})^t \quad (1.33)$$

By simply transposing  $(I_{ij})$  and changing the sign  $(E_{ij})$  is obtained.

The assumption used in deriving this result is the regularity of  $R_2$  which will now be proved.

Referring the mesh equation eq.(1.8) the last  $M$  columns of  $(R_{ij})$ , which make the minor matrix  $R_2$  are related to the branches of the resistances of  $R'$  group, the inductances and the current sources, or, in other word, the branches that are not those related to the columns of the matrix  $D_1$ . When  $D_1$  is regular the branches represented by the columns of  $D_1$  make a tree. In this case the remaining  $M$  branches make a cotree. According to a theorem in topology the mesh matrix of the cotree is regular. Therefore

$$\det R_2 \neq 0 \quad (1.34)$$

As the consequence eq.(1.33) is true in case the simulation is possible.

Eq.(1.33) is written for the network of Fig. 1.12 by using eq.(1.26). The input-output relation of the E - matrix circuit of this network is then

$$\begin{pmatrix} e_7 \\ e_8 \\ e_9 \\ e_{10} \\ e_{11} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 & -1 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & -1 & 0 & 0 & 0 & -1 \\ 0 & 0 & -1 & 0 & 0 & 0 \\ -1 & 1 & 1 & 1 & 1 & 0 \end{pmatrix} \begin{pmatrix} e_1 \\ e_2 \\ e_3 \\ e_4 \\ e_5 \\ e_6 \end{pmatrix} \quad (1.35)$$

## 1.8 Automatic Programming of Analog Computer by Digital Computer.

The previous sections have dealt with the general theory of the network simulation by the analog computer. As the result useful criteria for the possibility of the network simulation were obtained. The problem of the network simulation is however, not yet completely solved even when the possibility is identified. Although the sweep-out method for obtaining  $(I_{ij})$  and  $(E_{ij})$  is quite effective the manual computation is often painstaking especially when the network is large.

The author tried to obtain  $(I_{ij})$  and  $(E_{ij})$  from the connection matrix of the network automatically by means of the digital computer and completed a FORTRAN program for IBM 7090. This network simulation program is applicable to any

electrical network having up to 75 independent nodes and 150 branches. The structure of this program will now be described.

The data cards used for this program should be prepared so that the first card is punched with the following numbers in the format of ( 5I5 ).

number of independent nodes, number of branches,

number of voltage sources, number of capacitans, and number of resistances.

The data cards from the second are punched with the elements of the connection matrix columnwise, that is,  $D_{1j}$ ,  $D_{2j}$ , ...,  $D_{Nj}$ , in the format of ( 75I1 ) so that one card contains all elements of the connection matrix of a branch. In punching  $D_{ij}$ , the letter 2 is used instead of -1.

The flow chart of the program is shown in Fig. 1.13. After reading out the input data, letters of 2 in  $D_{ij}$  is changed into -1 and the connection matrix (  $D_{ij}$  ) is printed out. Then the necessary condition for the network

simulation is tested according to ineq.(1.19).

If this condition is not satisfied the computer prints following words and the computation ends.

THE SIMULATION OF THIS NETWORK IS IMPOSSIBLE (1.36)

When the condition is satisfied the sweeping-out of the connection matrix is executed. This is done from the first column to the  $N$  th column. At the  $j$  th column the computer looks for nonzero element in  $D_{ij}$  in which  $i$  is not less than  $j$ . When this is found in  $i$  th row the element of this row is exchanged with those of the  $j$  th row and all other non-zero elements of the  $j$  th column are erased. In case any non-zero elements are found in  $D_{ij}$  in which  $i$  is not less than  $j$ , computer asks if any other branches are eligible for the columns of  $D_1$  matrix. If the answer is "No" computer prints words of (1.36). If the answer is "Yes", that column is exchanged with the  $j$  th column and sweeping-out is performed. After the sweeping-out is

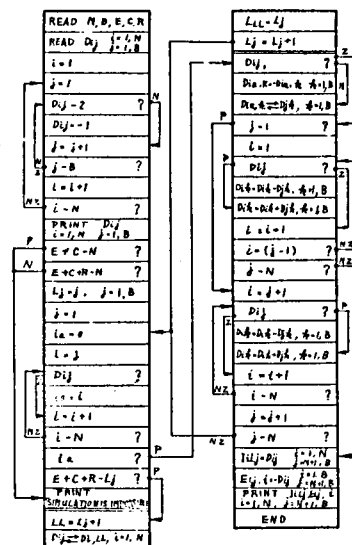


Fig. 1.13 Flow chart of FORTRAN program for calculating (  $I_{ij}$  ) and (  $E_{ij}$  ) from the connection matrix of given electrical network.

Table 1.1 - FORTRAN PROGRAM

```

2001 ANALOG COMPUTER CIRCUIT FOR THE NETWORK SIMULATION
DIMENSION ID(75,150),IDA(150),L(150),FMT(12)
9 READ INPUT TAPE 5,101,IMAX,JMAX,NE,NC,NR
PEAO INPUT TAPE 5,102,((ID(I,J),I=1,75),J=1,JMAX)
DO 12 J=1,JMAX
IF(ID(I,J)-2)10,11,11
10 GO TO 12
11 IC(I,J)=-1
12 CONTINUE
J1=1
18 IF(J1+19-JMAX)21,20,20
20 J2=JMAX
GO TO 22
21 J2=J1+19
22 I1=1
19 WRITE OUTPUT TAPE 6,103,(J,J=J1,J2)
IF(I1+29-IMAX)24,23,23
23 I2=IMAX
GO TO 25
24 I2=I1+29
25 DO 26 I=I1,I2
26 WRITE OUTPUT TAPE 6,104,I,(ID(I,J),J=J1,J2)
IF(I2-IMAX)27,28,28
27 I1=I1+30
GO TO 19
28 IF(J2-JMAX)29,30,30
29 J1=J1+20
GO TO 18
30 IF(NE+NC-IMAX)31,31,32
31 IF(NE+NC+NR-IMAX)32,33,33
32 WRITE OUTPUT TAPE 6, 105
GO TO 99
33 DO 34 J=1,JMAX
L(J)=J
DO 49 J=1,IMAX
IA=0
DO 36 I=J,IMAX
IF(IC(I,J))35,36,35
35 IA=I
36 CONTINUE
IF(IA)37,37,38
37 GO TO 51
38 IF(IC(IA,J))41,51,39
39 DO 40 K=1,JMAX
DO 41 ID(IA,K)=ID(IA,K)
41 DO 42 K=1,JMAX
IDA(K)=IC(IA,K)
ID(IA,K)=ID(J,K)
42 ID(J,K)=IDA(K)
IF(J-160,60,43
43 J3=J-1
DO 43 I=1,J3
IF(IC(I,J))44,44,46
44 DO 45 K=J,JMAX
ID(I,K)=ID(I,K)-IC(J,K)
45 GO TO 48
GO TO 48
46 DO 47 K=J,JMAX
47 ID(I,K)=IC(I,K)+ID(J,K)
48 CONTINUE
60 IF(J-IMAX)61,71,71
61 J4=J+1
DO 49 I=J4,IMAX
IF(ID(I,J))62,49,64
62 DO 63 K=J,JMAX
63 ID(I,K)=ID(I,K)-ID(J,K)
GO TO 48

```

```

20001 ANALOG COMPUTER CIRCUIT FOR THE NETWORK SIMULATION
64 DC 65 K=J,JMAX
65 ID(I,K)=ID(I,K)+ID(J,K)
49 CONTINUE
66 GO TO 71
51 IF(INE+NC+NR-L(J))52,52,53
52 GO TO 37
53 LL=L(J)+1
66 54 I=1,IMAX
66 ID(I)=ID(I,LL)
66 ID(I,LL)=ID(I,J)
54 ID(I,J)=ID(I)
66 L(LJ)=L(J)
66 L(J)=L(J)+1
66 GO TO 55
71 J1=JMAX+1
78 IF(J1+19-JMAX)81,80,80
80 J2=JMAX
66 GO TO 82
81 J2=J1+19
82 I1=1
79 WRITE OUTPUT TAPE 6,111,{L(J),J=J1,J2}
66 IF(I1+29-IMAX)84,81,83
83 I2=IMAX
66 GO TO 85
84 I2=I1+29
85 DO 86 I=I1,I2
86 WRITE OUTPUT TAPE 6,112,{L(I),{ID(I,J),J=J1,J2}
66 IF(I2-IMAX)87,88,88
87 I1=I1+30
66 GO TO 79
88 IF(J2-JMAX) 89,90,90
89 J1=J1+20
66 GO TO 78
90 J1=1
178 IF(J1+19-IMAX)181,180,180
180 J2=JMAX
66 GO TO 182
181 J2=J1+19
182 I1=IMAX+1
179 WRITE OUTPUT TAPE 6,113,{L(J),J=J1,J2}
66 IF(I1+29-JMAX)184,183,183
183 I2=JMAX
66 GO TO 185
184 I2=I1+29
195 DO 186 I=I1,I2
66 DC 199 K=J1,J2
199 ID(K)=-ID(K,I)
186 WRITE OUTPUT TAPE 6,114,{L(I),{ID(K),K=J1,J2}
66 IF(I2-JMAX)187,188,188
187 I1=I1+30
66 GO TO 179
188 IF(J2-IMAX)189,99,99
199 J1=J1+20
66 GO TO 178
101 FORMAT(5I5)
102 FORMAT(75I1)
103 FORMAT(1M1,14Z6HBRANCH 13,19I5)
104 FORMAT(1M0,3X4MNODE 13,9X20I5)
105 FORMAT(1M1,27Z44N THE SIMULATION OF THIS NETWORK IS IMPOSSIBLE)
111 FORMAT(1M1,13X7HCURRENT 13,19I5)
112 FORMAT(1M0,7HCURRENT 13,3X20I5)
113 FORMAT(1M1,13X7HVOLTAGE 13,19I5)
114 FORMAT(1M0,7HVOLTAGE 13,3X20I5)
99 GO TO 2
END(1,0,0,0,0,1,1,0,0,1,0,0,0,0,0)

```

completed for N columns the matrices ( Iij ) and ( Eij ) are printed. An outstanding function of this program is that the condition for the nework simulation is also tested in the course of the computation of ( Iij ) and ( Eij ).

Table 1.1 gives the complete program and Fig. 1.14 shows an example of the result for the network of Fig. 1.12.

CONNECTION MATRIX OF THE NETWORK IS

	BRANCH	1	2	3	4	5	6	7	8	9	10	11
NODE	1	-1	0	0	-1	0	0	0	0	0	0	0
NODE	2	0	1	-1	0	0	-1	1	-1	0	0	0
NODE	3	0	0	1	0	-1	0	0	1	0	1	0
NODE	4	0	-1	0	1	0	0	0	0	1	0	0
NODE	5	0	0	0	0	1	0	0	0	0	-1	1
NODE	6	0	0	0	0	0	1	-1	0	-1	0	0

I MATRIX OF ANALOG COMPUTER CIRCUIT IS

	CURRENT	7	8	9	10	11
CURRENT	1	0	0	0	0	1
CURRENT	2	-0	0	1	-0	-1
CURRENT	3	0	-1	0	-0	-1
CURRENT	4	-0	-0	-0	-0	-1
CURRENT	5	-0	-0	-0	1	-1
CURRENT	6	1	-0	1	-0	-0

E MATRIX OF ANALOG COMPUTER CIRCUIT IS

	VOLTAGE	1	2	3	4	5	6
VOLTAGE	7	-0	0	-0	0	0	-1
VOLTAGE	8	-0	-0	1	0	0	0
VOLTAGE	9	-0	-1	-0	0	0	-1
VOLTAGE	10	-0	0	0	0	-1	0
VOLTAGE	11	-1	1	1	1	1	0

Fig. 1.14 Result of Computation, by IBM 7090



## Chapter 2

### Study of Analog Computer Elements

#### 2.1 Introduction

In 1956 when the author began to work for the development of the dc analog computer at the Tsurumi Research Laboratory of the Tokyo - Shibaura Electric Co., Ltd only little was known of the detail of the design of the computer elements. As the author undertook the design of the largest scale analog computer in this country TOSAC-II he studied the design problem of analog computer and developed many analog computer elements. Those new elements were developed from the viewpoint of exploiting new way of applying the analog computer to the problems of electrical engineering in Toshiba Electric Co, Ltd. The developed computer elements, therefore, withstood the practical use and are now extensively used in the standard Toshiba analog computers.

The details of the design of some of these new computer elements are described in this chapter. Discussions on the static and dynamic accuracies of these elements are also described.

#### 2.2 Patch Board Design

The prepatch system of the analog computer programming is recognized useful and is almost indispensable to large scale machines. By preparing several patch boards the computer can solve different problems without interruption and a great deal of the machine time is saved.

The serious problem in designing patch board is the layout of the connection holes to which all input - and output - terminals of the whole elements of the computer are connected. As the space allowed for a patch board is limited the number of the connection holes is also limited. In designing the layout we have to satisfy two contradicting requirements, that is, any connection of the elements must be possible on the patchboard and also as many unnecessary connection holes as possible must be removed. The question is; what is the optimum layout of the connection holes of the patchboard, which makes possible any connection of the elements by using the limited number of the connection holes?

One solution adopted in many commercially available analog computers is the arrangement of special holes called multiple connector. This is a set of holes connected together. When one needs to connect a hole to more than one other holes he connects

these holes to the multiple connector . This way of connection is illustrated in Fig. 2.1

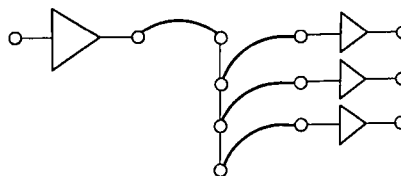


Fig. 2.1 Connection of computing elements by multiple connector

The use of the multiple connector solves the problem only partly, because it cannot be specified how many holes a multiple connector should have and how many multiple connectors are necessary to connect the computer elements on the patch board for any possible computer circuits.

Another attempt for the solution of this question is assigning more than one connecting holes to the output of each computer element. As the input terminal of the computer elements is never connected to more than one output terminal of the elements the connection hole for the input terminal need not be more than one, while several holes should be assigned to the output terminal. Fig. 2.2

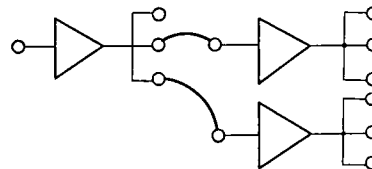


Fig. 2.2 Multiple output terminals are provided at computing element

shows an example of this type of patch board design . (The most commercial analog computers use the combined method of these two types). The layout of the REAC patch board <sup>15)</sup> is shown in Fig. 2.3.

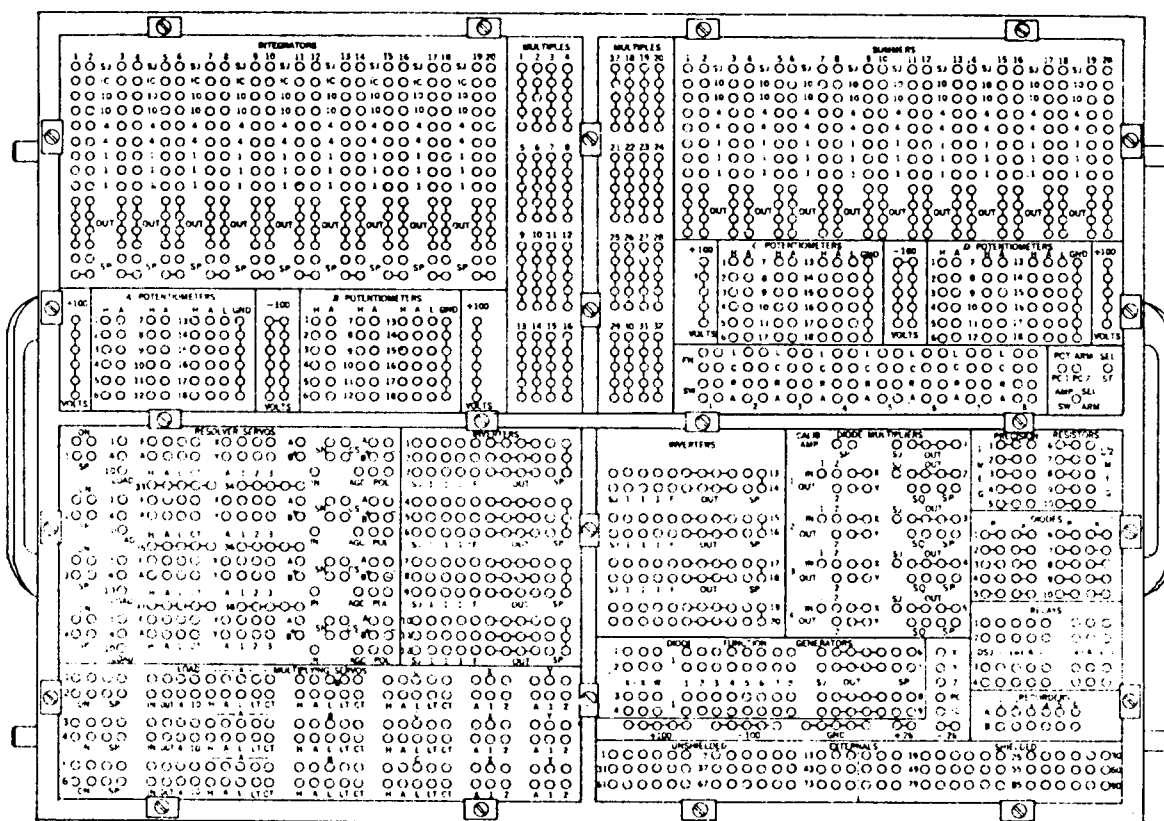
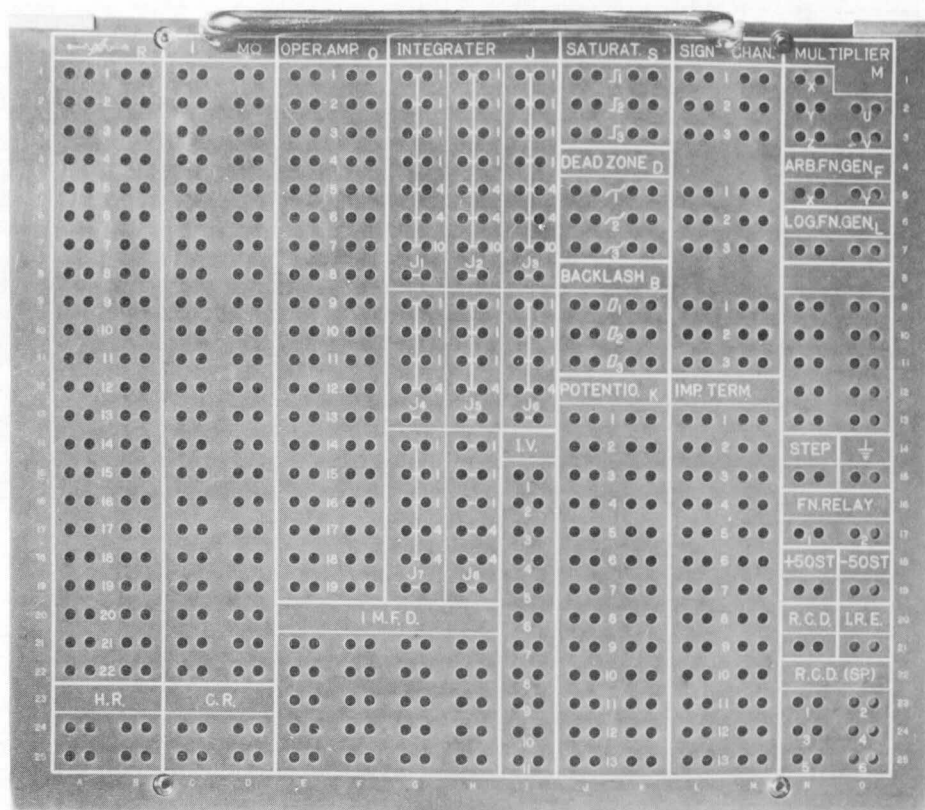
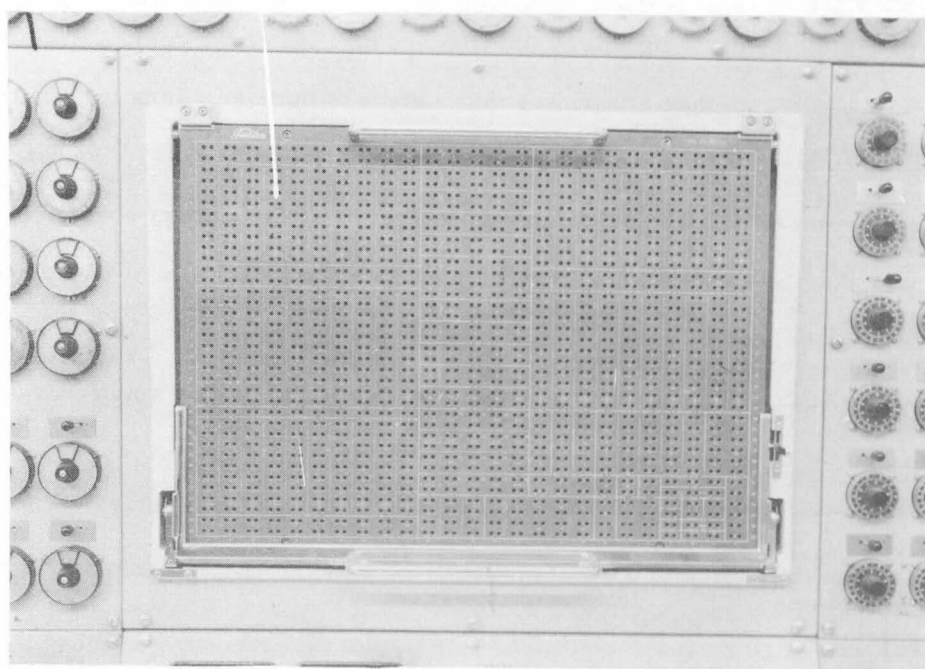


Fig. 2.3 Patch board layout of REAC



(a)



(b)

Fig. 2.5 Patch board layout of Toshiba analog computers.  
(a) TOSAC-1 (b) TOSAC-II

The patch board of the Toshiba Analog Computer designed by the author is different from those of the commercial machines. Before describing the design the problem of connecting  $n$  distinct points by wires is considered.

The minimum number of the wires connecting  $n$  points is  $n - 1$  as explained in Fig. 2.4. Let these wires be patch - cords.

Then they have two pins at each end .

Therefore there needs at least  $2( n - 1 )$

holes for  $n$  points to connect these

points by patch - cords.

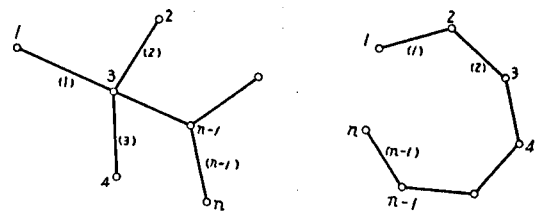


Fig. 2.4 Connecting  $n$  points by  $( n - 1 )$  lines.

When individual point has a pair of holes  $n$  points make  $2 n$  holes which are two more than are required. This is the principle of the patch board of the Toshiba Analog Computer. Namely two holes are assigned for all of the terminals of the computing elements. By this method any connection of the computer elements is possible. This method eliminates indefiniteness in determining the number of the multiple connectors and the number of holes of each of them. This method also provides a merit for the mechanical construction of the contact spring of the patch - bay as a double - sized spring may be used to connect a terminal of the computer element to the pins of the two holes of the patch - board. Fig. 2.5 shows the patch - boards of TOSAC - I and - II. Fig. 2.6 is an example of the connection of the computer circuit of TOSAC - II.

### 2.3 Computer for the Loading Effect Correction of the Potentiometer <sup>16)</sup>

The multiplication of a constant coefficient on the analog computer is done by the potentiometer. In the analog computer circuit the potentiometer is unavoidably loaded by the input impedances of the computer elements and produces an error in the multiplication factor. This is the loading effect of the potentiometer. The re-

sistance of the potentiometer to avoid the loading effect is not a favorable method because more output current of the operational amplifier is required. Increasing the input impedance of the computer elements cannot be the solution, too, as the precision of the large impedances is usually hard to maintain. The loading effect of the potentiometer should, therefore, be removed by the correction.

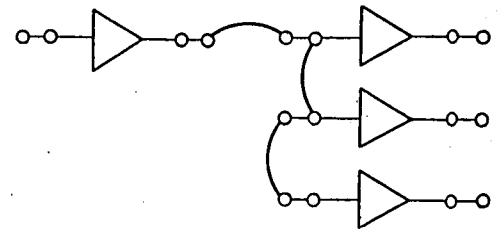


Fig. 2.6 Connection of computing elements which have a pair of connection holes both at input and output terminals.

The correction factor of a potentiometer loaded with a resistance of  $R$  ohms is given by the following formula.

$$F = \frac{R}{R + (1-a)ar} \quad (2.1)$$

Fig. 2.7 shows the relation of  $(1-F)a$  to  $a$  and  $R$ . One can use this chart to estimate the error of the multiplication factor due to the loading effect.

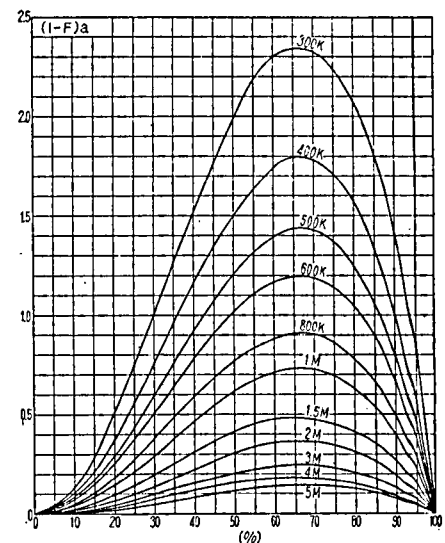


Fig. 2.7 Load effect characteristic of the potentiometer having total resistance of 50 k

The correction of the loading effect is often cumbersome even when it is correctable. The use of the chart of Fig. 2.7 or similar one is useful in few occasions.

To obtain the settings of the potentiometer with any load required for producing a multiplication factor the author has built an analog computer by servomechanisms. This is a very simple servomechanism yet is most useful in practical use. Fig. 2.8 is the schematic diagram of this load effect correction computer.

In Fig. 2.8  $P_1$  is potentiometer which is set to the desired multiplication factor and  $P_2$  is another potentiometer of which resistance is identical to those of the analog computer and is loaded by an adjustable resistance  $R$ . The potentiometer  $P_2$  is driven by a servomotor  $M$ . Same voltage is applied to  $P_1$  and  $P_2$ . The difference of the output voltages of  $P_1$  and  $P_2$  is amplified and is fed to the servo-amplifier driving the servomotor. As the result the setting of the potentiometer

$P_2$  is adjusted automatically so that the actual multiplication factor of  $P_2$  is equal to the multiplication factor of  $P_1$  which is set at a desired value. The dial of  $P_2$  shows the setting of the potentiometer to obtain the desired multiplication factor with the load  $R$ .

Fig. 2.9 shows the load effect correction computer installed in a large scale analog computer.

#### 2.4 Evaluation of the Time Delay Elements . 17) 18)

When solving the problems of nuclear reactors, chemical reactors or transmission lines on

the analog computer the time delay element which reproduces the input signal after a definite time is needed.

In general the phenomena of which input signal  $e_i(t)$  and output signal  $e_o(t)$  are described by the next equation

$$e_o(t) = e_i(t - \tau) \quad (2.2)$$

are the time delay and the element simulating this phenomenon is the time delay element.

The time delay element is one of the important element of the analog computer and various attempts have been done

to build accurate and versatile time delay elements. However, there is a lack of the criterion to evaluate these time delay elements with regard to their suitability to particular problems and the dynamic error. The author proposed to use a quantity which is the product of the maximum frequency of the signal and the maximum

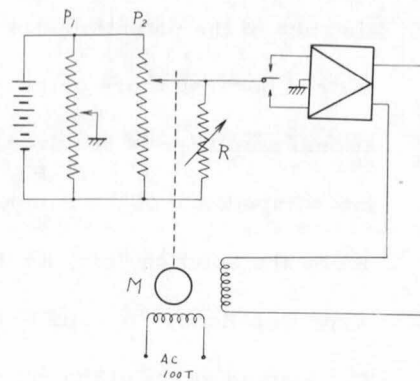


Fig. 2.8 Schematic diagram of the computer for the loading effect correction of the potentiometer.  $P_1$  is set at the desired multiplication factor and  $R$  is set at the load resistance.  $P_2$  then shows the required setting of the potentiometer.

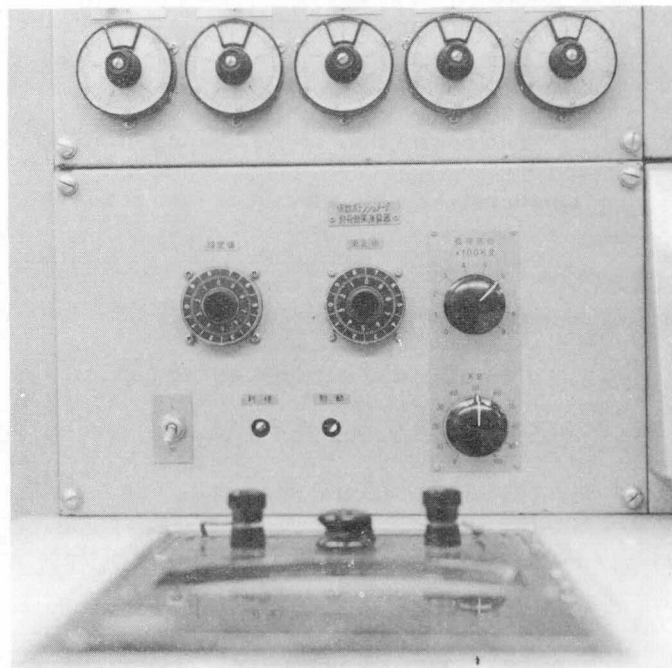


Fig. 2.9 Load effect computer built in a large analog computer.

delay time to evaluate the time delay element. In this section he derives this quantity for different types of the time delay elements.

The way of simulating the time delay is generally divided into two types. They are

(i) Analytical Approach <sup>19) 20) 21)</sup>

(ii) Synthetic Approach

The first approach uses the approximation of the transfer function of the time delay

$$G(S) = e^{-\tau s} \quad (2.3)$$

by passive elements and operational amplifiers. The second approach uses physical means exhibiting the property of the time delay.

#### 2.4.1 Analytical Approach

In the analytical approach to the simulation of the time delay passive elements and operational amplifiers are combined to approximate the transfer function  $e^{-\tau s}$ .

Let  $F(s)$  be an approximate function of  $e^{-\tau s}$ . The frequency response is expressed as

$$F(j\omega) = K(\omega\tau) e^{-j\phi(\omega\tau)} \quad (2.4)$$

Then following inequalities

$$|1 - K(\omega\tau)| < \epsilon \quad (2.5)$$

$$|\omega\tau - \phi(\omega\tau)| < \delta \quad (2.6)$$

are true only for a limited range of  $\omega\tau$  where  $\epsilon$  and  $\delta$  are permissible errors.

From in eq.(2.5) and in eq.(2.6) next inequality is obtained.

$$\omega\tau \leq A' \quad (2.7)$$

$$\text{or} \quad f.\tau \leq A$$

$$\text{where} \quad A' = 2\pi A$$

Ineq.(2.7) implies that to delay a signal of high frequency for a long time is difficult while slowly varying signal may be delayed for a considerable time. The quantity  $f.\tau$  is therefore usable to evaluate the performance of the time delay element of the analytical approach. The quantity of evaluation is calculated for several approximate formula of  $e^{-\tau s}$  in the remainder of this section.

#### (i) Linear Approximation

An approximation of  $e^{-\tau s}$  is as follows. <sup>21)</sup>

$$F(s) = \left( \frac{1 - \frac{\tau s}{2n}}{1 + \frac{\tau s}{2n}} \right)^n \quad (2.8)$$

For this approximation  $K(\omega\tau)$  is unity and  $\Phi(\omega\tau)$  is written

$$\Phi(\omega\tau) = 2n \tan^{-1} \frac{\omega\tau}{2n} \quad (2.9)$$

The phase error  $\frac{\delta}{\omega\tau} = \frac{\Phi(\omega\tau) - \omega\tau}{\omega\tau}$  is plotted against  $\omega\tau$  in Fig. 2.10. The phase error increases monotonically as  $\omega\tau$  increases. Expanding  $\Phi(\omega\tau)$  into power series of  $\omega\tau$

results

$$\Phi(\omega\tau) = \omega\tau - \frac{1}{3} \frac{(\omega\tau)^3}{(2n)^2} + \frac{1}{5} \frac{(\omega\tau)^5}{(2n)^4} \dots \quad (2.10)$$

The phase error  $\delta$  is then given approximately as

$$\delta = \omega\tau - \Phi(\omega\tau) \cong \frac{1}{3} \frac{(\omega\tau)^3}{(2n)^2} \quad (2.11)$$

The quantity of evaluation  $f \cdot \tau$  is derived from this equation as

$$A = f \cdot \tau = \frac{1}{\pi} \sqrt[3]{\frac{3}{2} n^2 \delta} \quad (2.12)$$

A is plotted against  $n$  for  $\delta = 0.1$  radian in Fig. 2.11.

The transfer function of eq. (2.8) for  $n=1$

$$\frac{E_o}{E_i} = \frac{1 - \frac{\tau s}{2}}{1 + \frac{\tau s}{2}}$$

is obtained by an analog computer circuit using two operational amplifiers. For  $n \neq 1$   $n$  stages of this computer circuit is cascaded. When  $n = 5$  ten operational amplifiers are needed. The figure of merit for  $n = 5$  is only 0.5.

(ii) Quadratic Approximation..

Quadratic form instead of the linear form gives better approximation. The quadratic approximation is

$$F(s) = \left\{ \frac{1 - \frac{\tau s}{2n} + \alpha \left( \frac{\tau s}{2n} \right)^2}{1 + \frac{\tau s}{2n} + \alpha \left( \frac{\tau s}{2n} \right)^2} \right\}^n \quad (2.13)$$

where  $\alpha$  is a correction factor to the linear approximation formula and will be determined to give best approximation.

The phase of this approximation is

$$\begin{aligned} \Phi(\omega\tau) &= 2n \tan^{-1} \left\{ \frac{\frac{\omega\tau}{2n}}{1 - \alpha \left( \frac{\omega\tau}{2n} \right)^2} \right\} \\ &\cong \omega\tau + \left( \alpha - \frac{1}{3} \right) \frac{(\omega\tau)^3}{(2n)^2} + \left( \alpha^2 - \alpha + \frac{1}{5} \right) \frac{(\omega\tau)^5}{(2n)^4} + \dots \end{aligned} \quad (2.14)$$

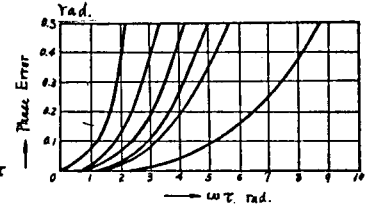


Fig. 2.10 Phase error of the approximate transfer function of time delay.

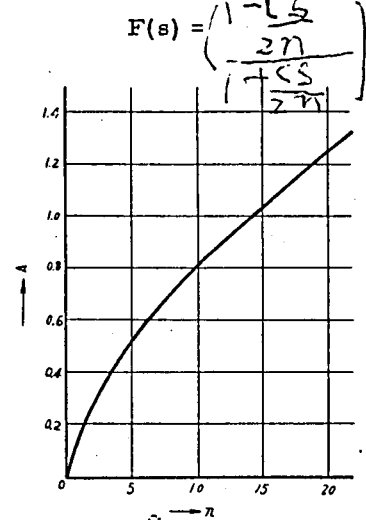


Fig. 2.11 Figure of merit of an approximate transfer function of time delay:

$$F(s) = \left( \frac{1 - \frac{\tau s}{2n}}{1 + \frac{\tau s}{2n}} \right)^n$$



The best approximation is attained when  $\alpha$  is selected

$$\alpha = \frac{1}{3} \quad (2.15)$$

The transfer function is then

$$F(s) = \left\{ \frac{1 - \frac{rs}{2n} + \frac{1}{3} \left( \frac{rs}{2n} \right)^2}{1 + \frac{rs}{2n} + \frac{1}{3} \left( \frac{rs}{2n} \right)^2} \right\}^n \quad (2.16)$$

and the phase error is

$$\delta = \omega\tau - \phi(\omega\tau) \cong \frac{1}{45} \frac{(\omega\tau)^5}{(2n)^4} \quad (2.17)$$

The figure of merit is then obtained as

$$A = f \cdot \tau = \frac{n}{\pi} \sqrt{\frac{45\delta}{2n}} \quad (2.18)$$

This quantity of evaluation is plotted against  $n$  for  $\delta = 0.1$  radian in Fig. 2.12.

Eq.(2.16) is known as Padé's approximation. 19)

#### 2.4.2 Sampled - Delay System.

The synthetic approach to the time delay element hitherto studied are

- (I) Capacitor Storage Method 22) 23)
- (II) Capacitor Shift Method 24) 25) 26)
- (III) Shift Register Method 27)
- (IV) Magnetic Recording. 28)

In the first three approaches the input signal is sampled by certain time interval and the sampled pulse signal is transported through memory cells. This system is named sampled - delay system in general. The principle of the sampled - delay system is explained by the schematic diagram of Fig. 2.13.

The sampling switch  $S$  interrupts input signal with the period of  $\Delta$  second and the memory cells  $D_1, D_2, \dots, D_n, \dots$  transfer their contents to the adjacent cells while  $S$  is open. The input signal is converted into a pulse train as shown in Fig. 2.14 in the memory cells.

Let the number of the memory cells be  $n$ , the time delay of the system is

$$\tau = n \Delta \text{ seconds.} \quad (2.19)$$

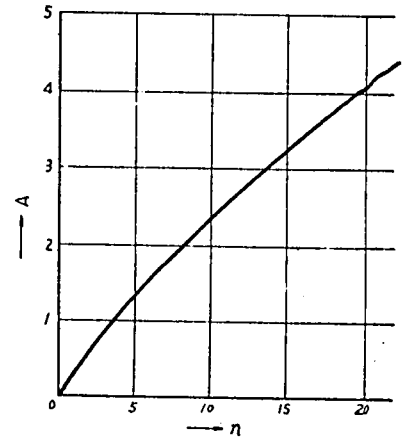


Fig. 2.12 Figure of merit of an approximate transfer function of time delay

$$F(s) = \left\{ \frac{1 - \frac{rs}{2n} + \frac{1}{3} \left( \frac{rs}{2n} \right)^2}{1 + \frac{rs}{2n} + \frac{1}{3} \left( \frac{rs}{2n} \right)^2} \right\}^n$$

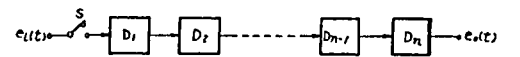


Fig. 2.13 Sampled - delay system for simulating time delay.

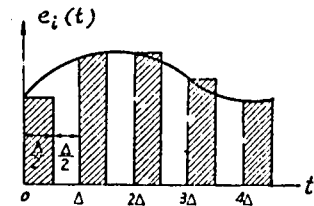


Fig. 2.14 Signals in sampled-delay system.

When the input signal is sinusoidal wave of the frequency  $f$  (c/s), that is

$$e_i(t) = E \sin 2\pi ft \quad (2.20)$$

and its one cycle is sampled  $m$  times, then

$$\frac{1}{f} = m \Delta \quad \text{seconds} \quad (2.21)$$

The sampling error increases as  $m$  decreases. Therefore  $m$  should be larger than some value to assure the accuracy. That is, there is a lower limit for  $m$ .

$$m \geq M \quad (2.22)$$

$M$  depends on the accuracy of the waveform reproducibility required. According to the sampling theorem  $M = 2$  is sufficient to reproduce the original waveform from the sampled - data provided ideal filter is used. In the present discussion, however, ideal filter is not considered and  $M = 2$  is much less than is required.

The number of the memory cells  $n$  is also limited from the economical reason and from the noise problem. Therefore

$$n \leq N \quad (2.23)$$

Eliminating  $\Delta$  from eq. (2.29) and (2.21) gives

$$f \cdot \tau = \frac{n}{m} \leq \frac{N}{M} \quad (2.24)$$

$N/M$  is the upper limit of  $f \cdot \tau$ , which is the figure of merit.

$$A = \frac{N}{M} \quad (2.25)$$

The adequacy of using  $f \cdot \tau$  to evaluate the time delay element is also proved in this case.

To increase  $A$   $N$  should be large and  $M$  should be small.  $N$  corresponds to the number of cascaded stages of the analytical approach. As each stage of analytical approach usually contains rather expensive operational amplifiers  $N$  is seldom taken more than five, while the memory cell of the sampled - delay system is usually simple and taking  $N$  as large as a hundred is not difficult.

The magnitude of  $M$  affects the accuracy of the reproduction of the waveform of the signal and has similar effect to the permissible phase error  $\phi$  of the analytical approach. By sampling the sinusoidal signal a staircase waveform of Fig. 2.15 is obtained. As this staircase signal

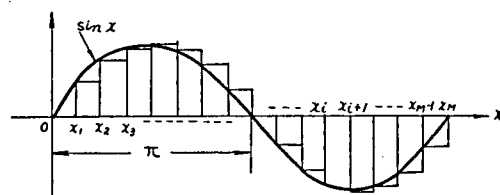


Fig. 2.15 Staircase approximation of sinusoidal wave.

loses higher - frequency components by passing through low - pass circuit it is

reasonable to define the distortion of the signal by the attenuation of the amplitude of the fundamental component of the staircase signal.

Dividing a cycle of the sinusoidal signal into  $M$  equal intervals at the points  $x_1, x_2, \dots, x_M$  which are

$$X_i = \frac{2\pi i}{M} \quad (i = 1, 2, \dots, M) \quad (2.26)$$

the staircase function is defined by the next equation.

$$f(x) = \sin x_i \quad (x_i \leq x < x_i + 1) \quad (2.27)$$

The sine component  $A_s$  and the cosine component  $A_c$  are obtained as follow.

$$\begin{aligned} A_s &= \frac{1}{\pi} \int_0^{2\pi} f(x) \sin x dx \\ &= \frac{1}{\pi} \sum_{i=0}^{M-1} \sin \frac{2\pi i}{M} \int_{\frac{2\pi i}{M}}^{\frac{2\pi(i+1)}{M}} \sin x dx \\ &= \frac{1}{2\pi} \sum_{i=0}^{M-1} \left[ \left(1 - \cos \frac{2\pi}{M}\right) \sin \frac{4\pi i}{M} + \sin \frac{2\pi}{M} \left(1 - \cos \frac{4\pi i}{M}\right) \right] \\ A_c &= \frac{1}{\pi} \int_0^{2\pi} f(x) \cos x dx \\ &= \frac{1}{\pi} \sum_{i=0}^{M-1} \sin \frac{\pi i}{M} \int_{\frac{2\pi i}{M}}^{\frac{2\pi(i+1)}{M}} \cos x dx \\ &= \frac{1}{2\pi} \sum_{i=0}^{M-1} \left[ \sin \frac{2\pi}{M} \sin \frac{4\pi i}{M} - \left(1 - \cos \frac{2\pi}{M}\right) \left(1 - \cos \frac{4\pi i}{M}\right) \right] \end{aligned} \quad (2.28)$$

By using the relations

$$\sum_{i=0}^{M-1} \cos \frac{4\pi i}{M} = 0 \quad (2.30)$$

and  $\sum_{i=0}^{M-1} \sin \frac{4\pi i}{M} = 0 \quad (2.31)$

$A_s$  and  $A_c$  are simplified resulting

$$A_s = \frac{M}{2\pi} \sin \frac{2\pi}{M} \quad (2.32)$$

$$A_c = -\frac{M}{2\pi} \left(1 - \cos \frac{2\pi}{M}\right), \quad (2.33)$$

The amplitude of the fundamental component of this staircase wave is therefore

$$\sqrt{A_s^2 + A_c^2} = \frac{M}{\pi} \sin \frac{\pi}{M} \quad (2.34)$$

and the amplitude error from the original sinusoidal wave is obtained as

$$\epsilon = 1 - \sqrt{A_s^2 + A_c^2} = 1 - \frac{M}{\pi} \sin \frac{\pi}{M} \quad (2.35)$$

In fig. 2.16  $\epsilon$  is plotted versus  $M$ . As will be seen in this figure the amplitude error is only 1.5% when  $M = 10$ . Substituting

$$M = 10 \quad (2.36)$$

$$\text{and } N = 100 \quad (2.37)$$

into eq.(2.25) the quantity of evaluation of the sampled delay system is calculated as

$$A = \frac{N}{M} = 10 \quad (2.38)$$

#### 2.4.3 Magnetic Tape Time Delay Elements

The second method of the synthetic approach is the magnetic tape recording. The principle

of the magnetic tape time delay element

is considered that of the sampled -

delay system. The figure of merit of this type of time delay element is calculated in a similar way.

The way of the modulation of the signal of the magnetic recording is either AM, FM, PWM or PCM. As AM lacks accuracy only FM, PWM and PCM are considered.

##### (i) Magnetic Recording by FM

The frequency modulation system converts the signal into the pulse train the repetition rate of which is proportional to the magnitude of the signal. The intervals between the adjoining pulses are the sampling interval. As the modulation factor in usual FM system is less than 50% the sampling rate is taken as  $f_0$ , the center frequency of the modulation. Then, sampling interval is

$$\Delta = 1/f_0 \quad (2.39)$$

and considering eq.(2.21) and eq.(2.22) leads to

$$\frac{1}{f} \geq \frac{M}{f_0} \quad (2.40)$$

Let  $k$  be the maximum modulation rate the maximum frequency of the pulses is

$$f_{\max} = (1 + k) \cdot f_0 \quad (2.41)$$

which is restricted by the packing density of the magnetic tape. When the frequency of the pulses are high the adjoining pulses are unable to discriminate. The maximum number of pulses in one centimeter of the magnetic tape, which are recorded and reproduced correctly, is called the packing density  $P$ . The minimum pulse interval

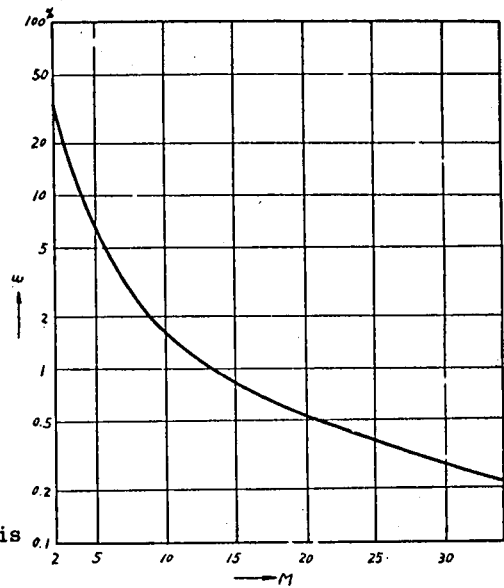


Fig. 2.16 Amplitude error vs. sampling rate  $M$ .

is  $1/p$  cm and the corresponding time interval is  $1/p V$  seconds where  $V$  is the tape speed in centimeters per second. The maximum frequency is then

$$f_{\max} = P V \quad (2.42)$$

Substituting eq. (2.42) into eq. (2.40) and into eq. (2.41), we obtain the following inequality.

$$f \leq \frac{1}{1+k} \frac{PV}{M} \quad (2.43)$$

On the other hand the delay time of the magnetic tape time delay element using endless tape has a practical limit. Let the length of the endless tape be  $L$  (cm), then

$$\tau \leq \frac{L}{V} \quad (2.44)$$

Eliminating  $V$  from eq. (2.43) and eq. (2.44) results

$$f \cdot \tau \leq \frac{1}{1+k} \frac{PL}{M}, \quad (2.45)$$

which gives the quantity of evaluation  $A$ .

$$A = \frac{1}{1+k} \frac{PL}{M} \quad (2.46)$$

The specifications of the endless tape time delay element built at Tokyo Institute of Technology are as follow: <sup>29)</sup>

$$\left. \begin{aligned} L &= 100 \quad (\text{cm}) \\ k &= 0.5 \\ M &= 10 \\ P &= 50 \quad (\text{pulses / cm}) \end{aligned} \right\} \quad (2.47)$$

The quantity of evaluation is then calculated as

$$A = 333 \quad (2.48)$$

From this calculation it is known that the magnetic tape time delay element is extremely superior to the analytical approach and the sampled - delay system.

## (II) Magnetic Recording by PWM.

In magnetic tape recording the pulse width modulation is preferable because this is free from the waw and the flutter of the magnetic tape. As the frequency of the sawtooth wave  $f_0$  is the sampling frequency of this system eq. (2.40) holds for this system, too. Using  $k$ , the maximum modulation rate, minimum pulse interval is written as

$$\frac{1-k}{2f_0} \quad \text{sec}$$

By considering the packing density, we obtain

$$f \leq \frac{1-k}{2} \frac{PV}{M} \quad (2.49)$$

For the endless tape of  $L$  (cm) long the quantity of evaluation is obtained as

$$A = \frac{1-k}{2} \frac{PL}{M} \quad (2.50)$$

Using the specifications of (2.47) this is calculated as

$$A = 125 \quad (2.51)$$

(iii) Magnetic Recording by PCM.

The pulse code modulation in magnetic tape recording may give the best accuracy.

Assume one word consists of  $N$  bits and the frequency of the pulse is  $f_0$  (c/s).

The sampling frequency is then  $f_0 / N$ . Then an inequality similar to ineq.(2.40) is obtained.

$$\frac{1}{f} \geq \frac{MN}{f_0} \quad (2.52)$$

Eq.(2.42) is written in this case as

$$f_0 = PV \quad (2.53)$$

From the above two equations results

$$f \leq \frac{PV}{MN} \quad (2.54)$$

Substituting this inequality into ineq.(2.42) the quantity of evaluation is obtained as

$$A = \frac{PL}{MN} \quad (2.55)$$

Let  $N = 7$  and using the specifications of (2.47) it is obtained that

$$A = 72 \quad (2.56)$$

#### 2.4.4 Concluding Remark

In the preceding discussions the adequacy of using  $f_{\max} \times \tau_{\max}$  as a quantity to evaluate the performance of the time delay elements has been testified. Whatever the type and the number of components of the time delay element are, it has a limited ability to delay quickly changing signal for a long time.

It should also be noted that we cannot extend the conclusion for any frequency of the signal and any length of the delay time. In magnetic tape recording time delay element, for instance, the frequency of the signal is limited by the tape speed as described by ineq.(2.42). The delay time is also limited. The similar circumstances exist for all types of the time delay elements, Therefore this figure of merit is not effective in extreme cases. The shadowed portion of Fig. 2.17 is the working domain

of the time delay element.

## 2.5 Variable Time Delay Element using Stroger Relay. 30)

A variable time delay element using Stroger relay was developed by the author for the purpose of using in the dynamic analysis of the nuclear power station. In a type of nuclear power reactors coolant flow rate is changed to control the reactor output. This effects the transport delay of the coolant system which plays an important part in the dynamic behaviour of the power reactor. To simulate the coolant system under this condition the delay time of the time delay element should be varied by a signal. The developed variable time delay element is of a very simple construction yet is of considerable accuracy.

Fig. 2.18 is the schematic diagram of the variable time delay element. The contacts of two banks of a Stroger relay are so connected that the contact of one bank is connected to that of another bank one step in advance. The capacitors are connected to these contacts.

The driving magnet of the Stroger relay is supplied with the frequency controlled current pulses by which the relay advances the contact at determined time interval.

The input signal is sampled by the moving contact of the bank A of the Stroger relay and stored on the capacitors. The stored signal is picked up by the moving contact of bank B at one step before the moving contact of bank A erases this stored signal in the next period, and is fed to the cathode follower. Let the time required to advance the moving contact one step be  $\Delta$  (sec) and the number of contacts of each bank of the Stroger relay be  $N$ , the time delay obtained is  $(N - 1) \Delta$  (sec).

The driving current pulses are produced by the circuit shown in Fig. 2.19. The repetition rate of the pulses is portional to the input voltage. Therefore the delay time of the variable time delay element is inversely proportional to this dc

voltage. The specifications of the built variable time delay element are given below:

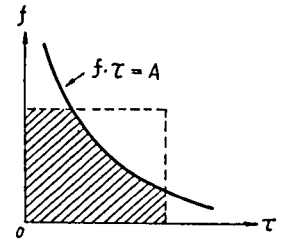


Fig. 2.17 Operational region of actual time delay element.

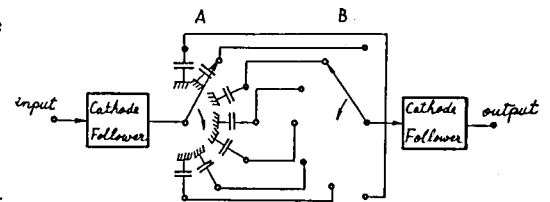


Fig. 2.18 Variable time delay element using Stroger relay

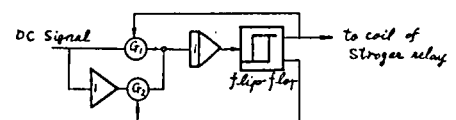


Fig. 2.19 Driving circuit of Stroger relay.

Number of Capacitor	25
Number of Contacts of a Bank	25
Number of Channel	2
Delay Time	1.25 seconds
	— 1 hour
Frequency Range	0 ~ 2 (c/s)
Linearity of Signal	0.5% F.S
Error of Delay Time Setting	1 %
Figure of Merit	2.5

## 2.6 Automatic Test Equipment of the Analog Computer 31) 32) 33)

### 2.6.1 Introduction

The increased utilization of the electronic analog computers necessarily demands larger and larger computer facilities. An analog computer consisting of a couple of hundreds of operational amplifiers is not unusual now. In these large scale analog computers the testing of the elements becomes a serious problem. As the analog computer is constructed by relatively sensitive elements such as high gain dc amplifiers, high precision resistances and potentiometers and precision servomechanisms, it is not always free from faults. The testing of the computer elements before using a large scale analog computer is almost unavoidable. But, as the testing of all elements at every operation of the computer is impossible, in most cases the improper function of the elements are found only after the obtained results are studied. Any person who has ever used analog computer may have experienced finding faulty elements in the computation circuit and replacing them by good ones after he has finished running the computer. He has to, then, repeat the whole computation. Should this happen the efficient utilization of the computer would be greatly suffered. Ideally before wiring the patch board connection the operator should be familiar with the condition of individual elements.

The automatic test equipment of the analog computer developed by the author serves for this purpose. This equipment facilitates the testing of all computer elements of a large scale analog computer in a couple of ten seconds. The principle of operation of the automatic test equipment is described below.

### 2.6.2 Automatic Testing of Analog Computers.

There are two different way<sup>1</sup> of testing the analog computer elements. The first



one is used in REAC - 400 series.<sup>34) 35) 36)</sup> The automatic testing system of REAC - 400 series checks both the faults of the computer elements and the program errors by using a set of relays to change all integraters into coefficient multipliers to compare nodal voltages with the calculated values. The second way of testing is to check all elements individually.<sup>37)</sup> This method of testing is reliable but requires a great deal of time and effort. Practically for large computers a portion of the computer is tested at a time.

The automatic test equipment of the author is of the second method. By this equipment precision and the zero drift of all integraters, adders, coefficient multipliers and operational amplifiers, the disconnection of the potentiometers and the instability of the operational amplifiers are checked in about twenty seconds and the detected improper operations of the elements are displayed on an neon tube panel.

The operator of the analog computer can wire patch - board connection referring this display. He can also check the operation of the computer elements which he has used after he has finished computer operation.

The whole view of the automatic test equipment of the analog computer is shown in Fig. 2.20, and the schematic diagram of the equipment is shown in Fig. 2.21. This is constructed by Stroger relays, comparater, discriminator, driving circuit of the Stroger relays, pulse generator, AND circuit, neon tube indicater and control circuit. The operations of these components are described below.

### 2.6.3 Principle of Operation<sup>38)</sup>

The output terminals of the computer elements are connected to the contact of a bank (bank A) of the stroger relay through patch - board. The contacts of another bank (bank B) of the Stroger relay are connected to the corresponding neon tube indicators of the display panel. The last bank (bank C) serves to generate control signals by which the Stroger relays are commutated and input signals are applied to the computer elements during the test.

Adders, integraters, coefficient multipliers and operational amplifiers are connected on the patch - board of the test equipment in a way shown in Fig. 2.22.

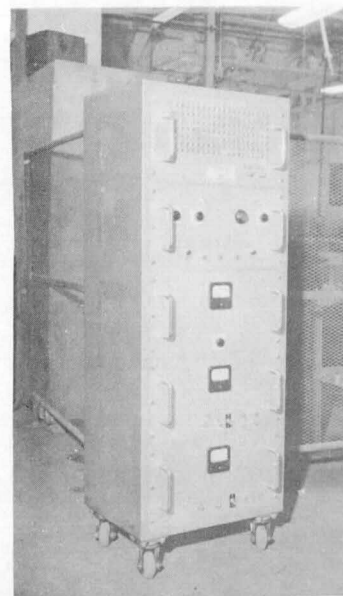


Fig. 2.20 Automatic test equipment of the analog computer

Multipliers and potentiometers are  
are connected as in Fig. 2.23.

The driving circuit of the Stroger relays generates a square wave which excites electromagnets of the relays and advances its moving contact one step for each period of the square wave. The Stroger relays having twenty five contacts in a bank are used. Their moving contacts rotate successively and twice and then stop. At the end of the first rotation the switch S closes and the moving contacts rotate for the second time. In this period of the second rotation the switches S' close. When the second rotation ends the test is finished.

During the first rotation of the moving contact switch S and S' are open and no signals are applied to the computer elements. If the operation of the element is normal its output will be zero. If there is any zero drift or oscillation of the computer element it is detected when the moving contact closes at this output and AND gate is opened to send a pulse to the neon tube indicator.

In the second period of rotation dc signals are applied to the input terminals of the computer elements so as to yield an identical output voltage. The output voltages of the computer elements are successively compared with a reference voltage by the comparater. If there is any difference the

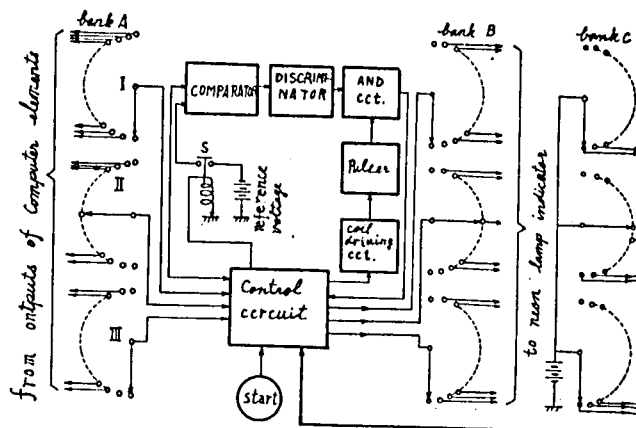


Fig. 2.21 Schematic diagram of the automatic test equipment of the analog computer

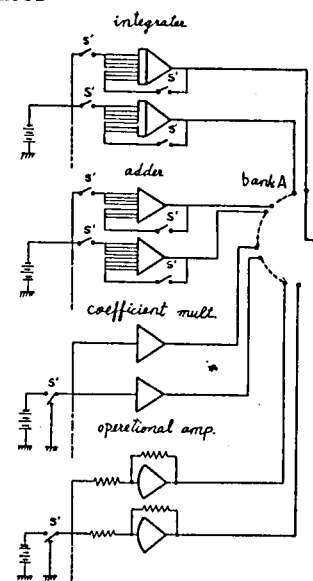


Fig. 2.22 Connection of integrators, adders, coefficient multipliers and operational amplifiers at the test.

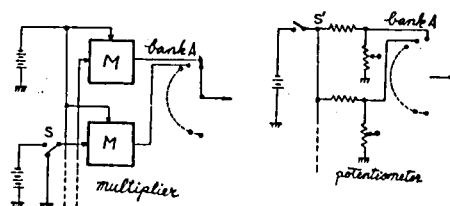


Fig. 2.23 Connection of multipliers and potentiometers at the test.

neon tube indicator is actuated. Faults such as the failure in power supply and the incorrect multiplication factor are detected at this second scanning period although they are undetectable in the first scanning period. Zero drift and oscillation of the operational amplifiers are undetectable in the second scanning period but are detected in the first scanning period. Potentiometers are tested only for the disconnection.

The comparater is a high gain chopper - stabilized dc amplifier followed by the discriminator. The input - output relation of the discriminator is shown in Fig. 2.24.

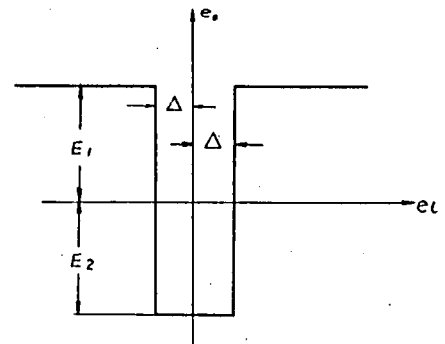


Fig. 2.24 Output - input relation of discriminator

As the moving contact of the bank B of the Stroger relay interrupts the circuits carrying voltages during the second scanning false pulses are produced at the moment of interruption which might cause misoperation of the neon indicator. The pulse generator and the AND circuit are prepared to prevent this misoperation. As the Stroger relay advances its moving contact at the moment when the current of the coil of the magnet discontinues, the false pulse is generated at the moment when the multivibrator output falls. Therefore the pulse obtained by differentiating the rising part of the multivibrator output is applied to the suppressor grid of 6AS6 to strobe the output of the discriminator which is applied to the control grid of this tube. The waveforms of various part of the circuit are shown in Fig. 2.25.

The circuit of the neon lamp indicators ought to be considerably simple because they are needed as many as the computer elements. The circuit is composed of two resistors, a neon tube and a germanium diode which are connected in a way shown in Fig. 2.26.

When the element under test is wrong a negative pulse is generated

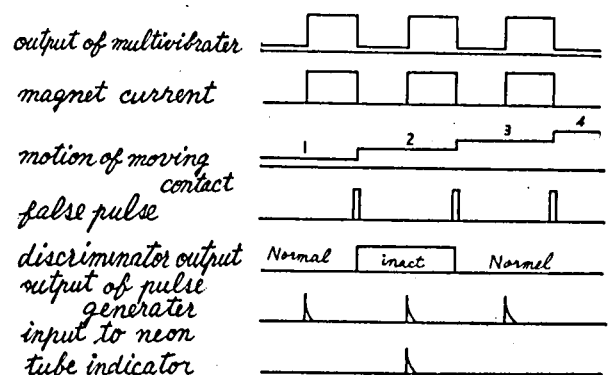


Fig. 2.25 Time chart of various signals.

from AND circuit, which forces to increase the voltage difference of the neon tube momentarily and fires it. Once this is fired the discharge potential decreases and the neon tube continues to fire after the negative pulse has extinguished. Fig. 2. 27 shows the panel of the neon tube indicator.

Finally the control circuit is composed of a group of relays which serve to interchange three Stroger relays, introduction of the reference voltage to the comparater and changing connection of the computer elements during the test.

#### 2.6.4 Concluding Remark.

The automatic test equipment of the analog computer developed by the author has no similar device in the world. By the use of this equipment the operation of the analog computer becomes more accessible as the precision of the computer elements are checked in a short while and the reliability of the solution of the computer greatly increases.

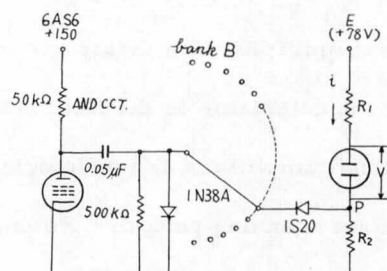


Fig. 2.26 AND circuit and Neon tube indicator

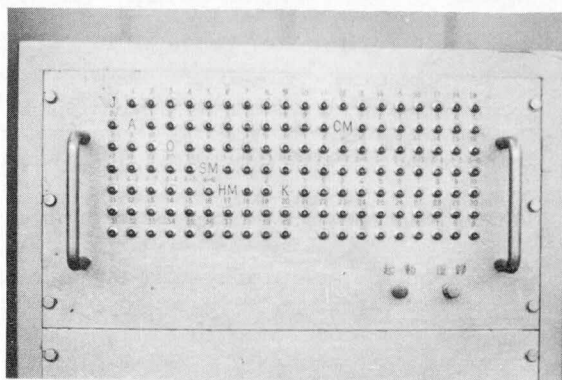


Fig. 2.27 Neon tube indicator panel

## Chapter 3

### Dynamics of Computing Servomechanisms.

#### 3.1 Introduction

The accuracy obtainable by the computing servomechanisms is far better than that by electronic nonlinear computer elements. The multipliers, the function generators and the resolvers are, in fact, the standard computer elements of the dc analog computer. However, because of the relatively slow response of the servomechanisms those computer elements should be carefully introduced into the analog computer circuits. The dynamics of the computing servomechanisms ought to be thoroughly understood before using them in actual computation. The dynamics of the computing servomechanisms introduce superfluous characteristic roots into the differential equation to be solved resulting an error in the waveform of the solution. The study of the dynamics of the computing servomechanisms is therefore important both for designing analog computer and for the analog computation.

Generally the computing servomechanisms are constructed by chopper circuit, ac servoamplifier and two - phase servomotor, the dynamics of which studied by the author are described in this chapter. In the first part of this chapter the frequency response of the overall system is studied with respect to the gear ratio, the speed - torque curve of the servomotor, the friction etc. This study, although not completely rigorous, gives a clear understanding of the dynamics and a design criterion of the computing servomechanisms.

In the second part the transfer function of the ac servoamplifier is studied. The transfer function based on the transient response of the carrier modulated system is derived and its feasibility for designing ac compensating network is shown.

The last part of the chapter is devoted to the study of the transfer function of chopper - modulated circuit. The chopper - modulated circuit is a periodically interrupted electrical network the mathematical treatment of which has been known

to be difficult. The author obtained the transient response of the chopper - modulated circuit using a small approximation and, by means of the  $z$  transform, derived the transfer function of this circuit.

### 3.2 Frequency Response

The bandwidth of the computing servomechanisms using two - phase servomotor is related to the gear ratio, the motor characteristics etc. An attempt of describing the bandwidth of the computing servomechanisms by the mechanical and electrical specifications was undertaken by T. Numakura.<sup>39)</sup> His formula tends to give a larger bandwidth than which is actually obtained and was not recommended for the design purpose. Another formula for the bandwidth of the servomechanisms was given by J. F. Truxal<sup>40)</sup>. His theory takes into account only the upper bound of the motor speed and is too simplified to describe the actual bandwidth.

The author has obtained the band - width from considering the phase plane of the feedback system based on the rigorous differential equation and the speed - torque curve of the servomotor.

The block diagram of the computing servo-

mechanism is shown in Fig. 3.1. The dc input signal is compared with the voltage from the follow - up potentiometer

and the difference is modulated by the chopper producing an ac error signal.

This ac error signal is amplified by the ac

servoamplifier the output of which excites control winding of the servomotor.

The servomotor drives the follow - up potentiometer via gear train.

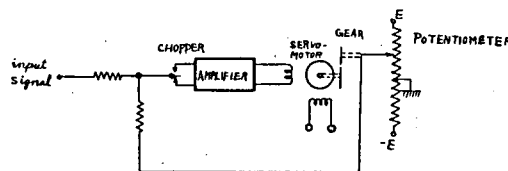


Fig. 3.1 Block diagram of computing servomechanisms.

As a first order approximation the frequency responses of the chopper - modulated circuit and of the servoamplifier are neglected. When a sinusoidal signal is applied at the input terminal of the servoamplifier the output voltage of the follow - up potentiometer must change sinusoidally. As the frequency of this sinusoidal signal increases the torque generated and the speed of the motor become unable to follow the change and the attenuation and the phase lag of the output voltage of the follow - up potentiometer result. The frequency range in which the servomechanism follows the input signal is the bandwidth of the system.

The computing servomechanism of Fig. 3.1 is considered as a simple system of Fig. 3.2 which is a load driven by a servomotor via a gear set. The differential equation of this system is written in terms of the angle of rotation  $\theta$ , the torque  $T$  and the moment of inertia  $J$  all at the load shaft.

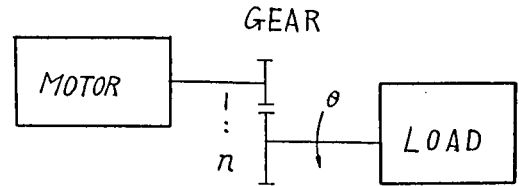


Fig. 3.2 Mechanical equivalence of computing servo-mechanisms.

Assume the load shaft is rotating sinusoidally at a frequency  $f$  (c/s) with an amplitude  $x$  (%), that is

$$\theta = \frac{\pi x}{100} \sin 2\pi f t, \quad (\text{radian}) \quad (3.1)$$

By differentiation we obtain

$$\frac{d\theta}{dt} = \frac{2\pi^2 x}{100} f \cos 2\pi f t \quad (3.2)$$

and

$$\frac{d^2\theta}{dt^2} = -\frac{4\pi^3 x}{100} f^2 \sin 2\pi f t \quad (3.3)$$

Denoting the speed of rotation of the motor by  $N_M$  gives

$$\frac{d\theta}{dt} = \frac{1}{n} \frac{2\pi}{60} N_M \quad (3.4)$$

where  $n$  is the gear ratio.

Now the equation of the motion of this system is written as

$$\frac{J}{g} \frac{d^2 \theta}{dt^2} = n T_M - T_F \operatorname{sgn} \left( \frac{d\theta}{dt} \right) \quad (3.5)$$

where  $T_M$  : Torque generated by motor (gr. cm)  
 $T_F$  : Torque due to friction at load shaft (gr. cm)  
 $J$  : Moment of inertia at load shaft (gr. cm<sup>2</sup>)

which is

$$J = J_L + J_G + n^2 J_M \quad (3.6)$$

$J_L$  : Moment of inertia of load (gr. cm<sup>2</sup>)  
 $J_G$  : Moment of inertia of gear at load shaft ( " )  
 $J_M$  : Moment of inertia of the rotor of the motor ( " )  
 $g$  : acceleration of gravity = 980 (cm/sec<sup>2</sup>)

Eq. (3.2) and eq. (3.4) result the relation

$$\frac{1}{n} \frac{2\pi}{60} N_M = \frac{2\pi^2 f x}{100} \cos 2\pi f t$$

From eq. (3.3) and eq. (e. 5) we obtain

$$\left\{ n T_M - T_F \operatorname{sgn} \left( \frac{d\theta}{dt} \right) \right\} = - \frac{4\pi^2 x}{100 g} f^2 \sin 2\pi f t$$

The above two equations are written in the next forms.

$$\begin{cases} N_M = N_o \cos 2\pi f t \\ T_M = \frac{1}{n} T_F \operatorname{sgn} (N_M) - T_o \sin 2\pi f t \end{cases} \quad (3.7)$$

$$T_M = \frac{1}{n} T_F \operatorname{sgn} (N_M) - T_o \sin 2\pi f t \quad (3.8)$$

where

$$N_o = \frac{60\pi}{100} n x f \quad (3.9)$$

$$T_o = \frac{4\pi^3 x}{100 g n} J f^2 \quad (3.10)$$

The velocity of rotation and the torque are limited by the speed - torque characteristic of the two - phase servomotor, which is shown in Fig. 3.3.

Eliminating  $\cos 2\pi f t$  and  $\sin 2\pi f t$  from eq. (3.7) and eq. (3.8) leads-

to the equation

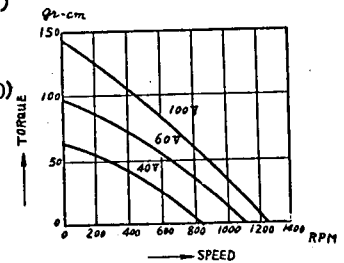


Fig. 3.3 Control characteristic of typical two - phase servo motor.



$$\left( \frac{N_M}{N_0} \right)^2 + \frac{1}{T_0^2} \left\{ T_M - \frac{T_F}{n} \operatorname{sgn}(N_M) \right\}^2 = 1 \quad (3.11)$$

which gives a locus in the phase plane. This locus is a discontinuous ellipse as shown by curve B of Fig. 3.4. Curve A in the same figure is the speed torque curve of the two - phase servomotor at the maximum excitation. Should curve B lie inside curve A the existence of this locus is permitted, or eq.(7) and eq.(8) are satisfied by this system and the motion of the potentiometer is purely sinusoidal.

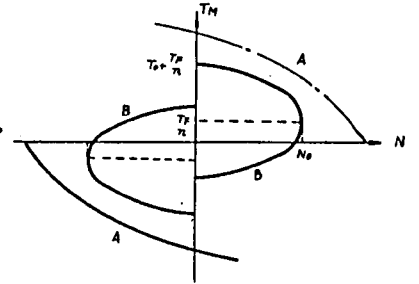


Fig. 3.4 Speed - torque curve at the maximum excitation (A) and phase plane locus of servo-mechanism in sinusoidal motion (B)

The principal axes of this ellipse are  $N_0$  and  $T_0$ . When gear ratio  $n$  is small  $N_0$  is small and  $T_0$  is large. Under this condition, the ellipse B penetrates curve A as shown in Fig. 3.5 (a). In contrary, when  $n$  is large the ellipse expands laterally penetrating curve A in a way shown in Fig. 3.5 (b). The former case may be considered the torque saturation while the latter may be considered the speed saturation.

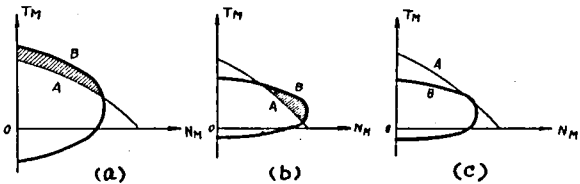


Fig. 3.5 Relative position of speed - torque curve (A) and phases plane locus (B). (a) torque saturation which occurs when gear ratio is small. (b) speed saturation which occurs when gear ratio is large. (c) case of optimum gear ratio.

To be more quantitative the relation between the gear ratio and the maximum followable frequency at an amplitude  $x$  is investigated. The maximum frequency is obtained when the ellipse B contacts curve A as shown in Fig. 3.5 (c).

For ease of computation the speed - torque curve of the two - phase servomotor at the maximum excitation is substituted by a straight line connecting static torque  $T_1$  and no load speed  $N_1$ . This is shown in Fig. 3.6. The torque and the speed on this straight line are described by the next equation

$$T_M = T_1 - \frac{T_1}{N_1} N_M, \quad (N_M > 0) \quad (3.12)$$

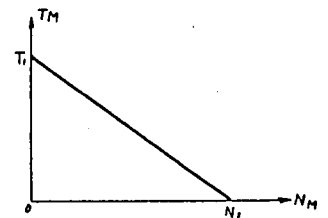


Fig. 3.6 Approximate speed torque curve at the maximum excitation.

Substituting eq.(3.12) into eq.(3.11) results

$$\left( \frac{T_0^2}{N_0^2} + \frac{T_1^2}{N_1^2} \right) N_0^2 + 2 \frac{T_1}{N_1} \left( \frac{T_F}{n} - T_1 \right) N_0 + \left( \frac{T_F}{n} - T_1 \right)^2 - T_0^2 = 0 \quad (3.13)$$

In order that the ellipse is inside the speed torque curve of eq.(3.12), eq.(3.13)

ought to have no real root. The discriminant should not, therefore, be positive.

$$D = \left( \frac{T_1}{N_1} \right)^2 \left( \frac{T_F}{n} - T_1 \right)^2 - \left( \frac{T_0^2}{N_0^2} + \frac{T_1^2}{N_1^2} \right) \left\{ \left( \frac{T_F}{n} - T_1 \right)^2 - T_0^2 \right\} \leq 0$$

This is rewritten as

$$\left( \frac{T_0}{T_1} \right)^2 + \left( \frac{N_0}{N_1} \right)^2 \leq \left( 1 - \frac{1}{n} \frac{T_F}{T_1} \right)^2 \quad (3.14)$$

The equality holds when ellipse and speed - torque curve are in contact. Replacing

$N_0$  and  $T_0$  of ineq.(3.14) by those of eq.(3.9) and eq.(3.10) and rearranging, we

finally obtain

$$f \leq \frac{g T_1}{4 \pi^2 \left( n J_M + \frac{J_L + J_G}{n} \right)} \left[ \left\{ \frac{1}{4} \left( \frac{60}{N_1} \right)^4 n^4 + \frac{10^4}{x^2} \left( \frac{4 \pi}{g T_1} \right)^2 \left( n J_M + \frac{J_L + J_G}{n} \right) \left( 1 - \frac{T_F}{n T_1} \right)^2 \right\} - \frac{1}{2} \left( \frac{60}{N_1} \right)^2 n^2 \right]^{\frac{1}{2}} \quad (3.15)$$

The frequency  $f$  satisfying the equality in the above ineq.(3.15) is plotted versus  $n$

in Fig. 3.7, where the following data are assumed.

$$\begin{aligned} T_1 &= 400 && \text{gr.cm} \\ J_L + J_G &= 1200 && \text{gr.cm}^2 \\ J_M &= 50 && \text{gr.cm}^2 \\ N_1 &= 1500 && \text{RPM} \\ T_F &= 200 && \text{gr.cm} \end{aligned}$$

The frequency satisfying the ineq.(3.15) is in the left

side of the curve of Fig. 3.7. The gear ratio is divided into three domains by this curve. In the domain above the curve the speed saturation takes place. In the domain under the curve the torque saturation takes place. The third domain which lies between the above two gives the gear ratio which

makes the servomechanism being able to follow the sinusoidal signal of which frequency is given on the abscissa. It is quite reasonable that the region of followable frequency increases as amplitude  $x$  decreases.

The maximum obtainable frequency  $f_{\max}$  for a given amplitude  $x$  (%) is represented by the peak of the curve of Fig. 3.7. This frequency is calculated in a following way.

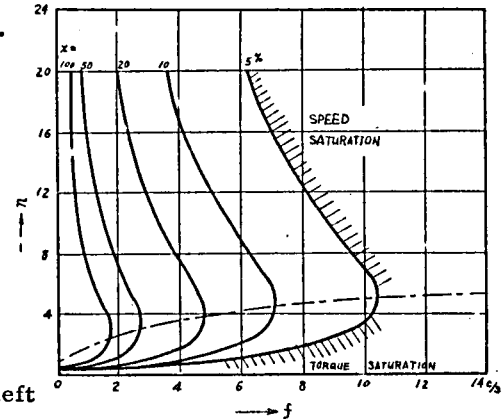


Fig. 3.7 Optimum gear ratio as a function of followable frequency and amplitude in case  $T_1 = 400$  gr.cm,  $J_L + J_G = 1200$  gr.cm<sup>2</sup>,  $J_M = 50$  gr.cm<sup>2</sup>,  $N_1 = 1500$  rpm and  $T_F = 200$  gr.cm.



dc signal is fed into conventional dc compensating circuit and then modulated again. The most usual way of the compensation is, however, the ac compensation shown in Fig. 3.8(b) as this is more economical.<sup>44)</sup> When an ac compensation network is included in ac servoamplifier its transfer function is no longer simple. Should the transfer function of the carrier - modulated system be explicitly formulated the ac compensation will be more feasible and the ac servomechanisms will be able to find more applications. In this chapter the transfer function of ac servomechanisms is formulated in a similar form of conventional transfer function.

The transfer function of the carrier - modulated system has not been given in definite form. That is, instead of transfer function a simple frequency response considering the envelope of carrier modulated signal has been used to discuss the dynamics of the ac servo systems. The measurement of the transfer function of the carrier - modulated system is therefore done by using sinusoidal signal to modulate carrier wave and observing the amplitude and the phase of the slightly distorted modulated wave.

The author had been suspicious of this method of discussing the envelope of the carrier - modulated signal and derived the transfer function of the system from the transient response. As the result he concluded the <sup>re</sup> previous method based on the envelope of the signal is not adequate and the relation of the demodulated signal to the modulating signal should be considered. The method of calculating the frequency response of the carrier modulated system by D Morris<sup>45)</sup> considers this relation and is valid from the authors view point.

### 3.3.2 Transfer Function Calculation

The forward elements of the ac servomechanisms is shown in Fig. 3.9. In this diagram  $e(t)$  and  $m(t)$  are dc signals and  $\theta_i(t)$  and  $\theta_o(t)$  are modulated signals. The present interest is in the transfer function of converting  $e(t)$  into  $m(t)$ .

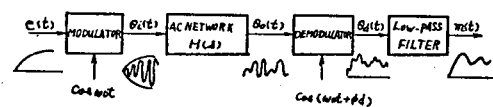


Fig. 3.9 Forward elements of ac servomechanisms

$e(t)$  is considered an arbitrary function of time and the corresponding output  $m(t)$  is to be obtained. Let  $\omega_c$  the angular frequency of the carrier signal, then the output of the modulator is written

$$\theta_i(t) = e(t) \cos \omega_o t \quad (3.20)$$

Denoting the Laplace transform of  $\theta_i(t)$  and  $e(t)$  by  $\Theta_i(s)$  and  $E(s)$  respectively, we obtain

$$\Theta_i(s) = \int_0^{\infty} \theta_i(t) e^{-st} dt = \frac{1}{2} [E(s + j\omega_o) + E(s - j\omega_o)] \quad (3.21)$$

If  $H(s)$  is the transfer function of ac network concerning dc signal the Laplace transform of the output of this network  $\Theta_o(s)$  is given by

$$\Theta_o(s) = H(s) \cdot \Theta_i(s) = \frac{1}{2} H(s) [E(s + j\omega_o) + E(s - j\omega_o)] \quad (3.22)$$

The inverse Laplace transform of  $\Theta_o(s)$  is

$$\theta_o(t) = \frac{1}{2\pi j} \int_{-j\infty}^{j\infty} \frac{1}{2} H(s) [E(s + j\omega_o) + E(s - j\omega_o)] e^{st} ds \quad (3.23)$$

To perform this integration  $H(s)$  is separated into the even and the odd functions; that is,

$$H(s) = M(s) + N(s) \quad (3.23)$$

$$M(s) = M(-s) \quad (3.24)$$

$$N(s) = -N(-s) \quad (3.25)$$

$M(s)$  and  $N(s)$  are expanded in the following alternative forms,

$$\begin{aligned} M(s) &= M(-j\omega_o + s + j\omega_o) \\ &= M\{j\omega_o - (s + j\omega_o)\} \\ &= M(j\omega_o) - (s + j\omega_o) M'(j\omega_o) + \frac{1}{2!} (s + j\omega_o)^2 M''(j\omega_o) + \\ &\quad \dots + \frac{(-1)^n}{n!} (s + j\omega_o)^n M^{(n)}(j\omega_o) + \dots \end{aligned} \quad (3.26)$$

$$\begin{aligned} N(s) &= N(-j\omega_o + s + j\omega_o) \\ &= -N\{j\omega_o - (s + j\omega_o)\} \\ &= -N(j\omega_o) + (s + j\omega_o) N'(j\omega_o) - \frac{1}{2!} (s + j\omega_o)^2 N''(j\omega_o) + \\ &\quad \dots + \frac{(-1)^{n-1}}{n!} (s + j\omega_o)^n N^{(n)}(j\omega_o) + \dots \end{aligned} \quad (3.27)$$

$$\begin{aligned} M(s) &= M\{j\omega_o + (s - j\omega_o)\} \\ &= M(j\omega_o) + (s - j\omega_o) M'(j\omega_o) + \frac{1}{2!} (s - j\omega_o)^2 M''(j\omega_o) \\ &\quad + \dots + \frac{1}{n!} (s - j\omega_o)^n M^{(n)}(j\omega_o) + \dots \end{aligned} \quad (3.28)$$

$$\begin{aligned} N(s) &= N\{j\omega_o + (s - j\omega_o)\} \\ &= N(j\omega_o) + (s - j\omega_o) N'(j\omega_o) + \frac{1}{2!} (s - j\omega_o)^2 N''(j\omega_o) \\ &\quad + \dots + \frac{1}{n!} (s - j\omega_o)^n N^{(n)}(j\omega_o) \end{aligned} \quad (3.29)$$

Using these formulae  $H(s)$  is expanded into the following following alternative forms

$$\begin{aligned} H(s) &= \{M(j\omega_o) - N(j\omega_o)\} - (s + j\omega_o) \{M'(j\omega_o) - N'(j\omega_o)\} \\ &\quad + \frac{1}{2!} (s + j\omega_o)^2 \{M''(j\omega_o) - N''(j\omega_o)\} + \dots \end{aligned}$$

$$+ \frac{(-1)^n}{n!} (s+j\omega_0)^n \{M^{(n)}(j\omega_0) - N^{(n)}(j\omega_0)\} + \dots \quad (3.30)$$

$$H(s) = \{M(j\omega_0) + H(j\omega_0)\} + (s-j\omega_0) \{M'(j\omega_0) + N'(j\omega_0)\} \\ + \frac{1}{2!} (s-j\omega_0)^2 \{M''(j\omega_0) + N''(j\omega_0)\} + \dots \\ + \frac{1}{n!} (s-j\omega_0)^n \{M^{(n)}(j\omega_0) + N^{(n)}(j\omega_0)\} + \dots \quad (3.31)$$

As  $M(s)$  is an even function and  $N(s)$  is an odd function it is shown that

$$M(j\omega_0), M''(j\omega_0), \dots, M^{(2n)}(j\omega_0), \dots, N'(j\omega_0), N^{(3)}(j\omega_0), \dots, \\ N^{(2n+1)}(j\omega_0), \dots \quad (3.32)$$

are real numbers and

$$M'(j\omega_0), M^{(3)}(j\omega_0), \dots, M^{(2n+1)}(j\omega_0), \dots, N(j\omega_0), N''(j\omega_0), \dots, \\ N^{(2n)}(j\omega_0), \dots \quad (3.33)$$

are imaginary numbers, hence following relations exist.

$$\left. \begin{aligned} M^{(2n)}(j\omega_0) - N^{(2n)}(j\omega_0) &= \overline{M^{(2n)}(j\omega_0) + N^{(2n)}(j\omega_0)} \\ M^{(2n+1)}(j\omega_0) - N^{(2n+1)}(j\omega_0) &= -\overline{M^{(2n+1)}(j\omega_0) + N^{(2n+1)}(j\omega_0)} \end{aligned} \right\} \quad (3.34)$$

Introducing real numbers  $C_n$  and  $\phi_n$ , these are written as

$$\left. \begin{aligned} M^{(2n)}(j\omega_0) - N^{(2n)}(j\omega_0) &= C_{2n} e^{j\phi_{2n}} \\ M^{(2n+1)}(j\omega_0) - N^{(2n+1)}(j\omega_0) &= jC_{2n+1} e^{j\phi_{2n+1}} \\ M^{(2n)}(j\omega_0) + N^{(2n)}(j\omega_0) &= C_{2n} e^{-j\phi_{2n}} \\ M^{(2n+1)}(j\omega_0) + N^{(2n+1)}(j\omega_0) &= jC_{2n+1} e^{-j\phi_{2n+1}} \end{aligned} \right\} \quad (3.35)$$

Substituting these formulae into eq.(3.30) and eq.(3.31), we obtain the integrand of eq.(3.23) in the following form.

$$\begin{aligned} \frac{1}{2} H(s) \{E(s+j\omega_0) + E(s-j\omega_0)\} &= \frac{1}{2} C \cdot \{e^{j\phi_0} E(s+j\omega_0) + e^{-j\phi_0} E(s-j\omega_0)\} \\ &+ \frac{C_2}{2!} \{(s+j\omega_0) e^{j\phi_2} E(s+j\omega_0) - (s-j\omega_0) e^{-j\phi_2} E(s-j\omega_0)\} \\ &+ \frac{C_2}{2 \cdot 2!} \{(s+j\omega_0)^2 e^{j\phi_2} E(s+j\omega_0) + (s-j\omega_0)^2 e^{-j\phi_2} E(s-j\omega_0)\} + \dots \\ &+ \frac{C_{2n}}{2 \cdot (2n)!} \{(s+j\omega_0)^{2n} e^{j\phi_{2n}} E(s+j\omega_0) + (s-j\omega_0)^{2n} e^{-j\phi_{2n}} E(s-j\omega_0)\} \\ &+ \frac{C_{2n+1}}{j 2 \cdot (2n+1)!} \{(s+j\omega_0)^{2n+1} e^{j\phi_{2n+1}} E(s+j\omega_0) - (s-j\omega_0)^{2n+1} e^{-j\phi_{2n+1}} E(s-j\omega_0)\} + \dots \end{aligned} \quad (3.36)$$

Using the relations

$$\left. \begin{aligned} \int_0^\infty e(t) \cos(\omega_0 t + \phi) e^{-st} dt &= \frac{1}{2} \{e^{j\phi} E(s+j\omega_0) + e^{-j\phi} E(s-j\omega_0)\} \\ \int_0^\infty e(t) \sin(\omega_0 t + \phi) e^{-st} dt &= \frac{1}{2j} \{e^{j\phi} E(s+j\omega_0) - e^{-j\phi} E(s-j\omega_0)\} \end{aligned} \right\} \quad (3.37)$$

the integration of eq.(3.23) is performed resulting  $\theta_o(t)$  as

$$\begin{aligned} \theta_o(t) &= C_0 e(t) \cos(\omega_0 t + \phi_0) + C_1 e'(t) \sin(\omega_0 t + \phi_1) \\ &+ \frac{1}{2!} C_2 e''(t) \cos(\omega_0 t + \phi_2) + \dots + \frac{1}{(2n)!} C_{2n} e^{(2n)}(t) \cos(\omega_0 t + \phi_{2n}) \\ &+ \frac{1}{(2n+1)!} C_{2n+1} e^{(2n+1)}(t) \sin(\omega_0 t + \phi_{2n+1}) + \dots \end{aligned} \quad (3.38)$$

The output of the demodulator  $\theta_d(t)$  is

$$\begin{aligned} \theta_d(t) &= \theta_o(t) \cos(\omega_0 t + \phi_d) \\ &= \frac{1}{2} C_0 e(t) \{\cos(\phi_0 - \phi_d) + \cos(2\omega_0 t + \phi_0 + \phi_d)\} \\ &+ \frac{1}{2} C_1 e'(t) \{\sin(\phi_1 - \phi_d) + \sin(2\omega_0 t + \phi_1 + \phi_d)\} \\ &+ \frac{1}{2 \cdot 2!} C_2 e''(t) \{\cos(\phi_2 - \phi_d) + \cos(2\omega_0 t + \phi_2 + \phi_d)\} + \dots \end{aligned}$$

$$\begin{aligned}
& + \frac{1}{2 \cdot (2n)!} C_{2n} e^{(2n)}(t) \{ \cos(\phi_{2n} - \phi_d) + \cos(2\omega_0 t + \phi_{2n} + \phi_d) \} \\
& + \frac{1}{2(2n+1)!} C_{2n+1} e^{(2n+1)}(t) \{ \sin(\phi_{2n+1} - \phi_d) + \sin(2\omega_0 t + \phi_{2n+1} + \phi_d) \} \\
& + \dots \dots \dots
\end{aligned} \tag{3.39}$$

when the frequency included in  $e(t)$ ,  $e'(t)$ , ..... is less than  $f_0$  the output signal of the low-pass filter is

$$\begin{aligned}
m(t) = & \frac{1}{2} C_0 e(t) \cos(\phi_0 - \phi_d) + \frac{1}{2} C_1 e'(t) \sin(\phi_1 - \phi_d) \\
& + \frac{1}{2 \cdot 2!} C_2 e''(t) \cos(\phi_2 - \phi_d) + \dots \dots \dots \\
& + \frac{1}{2 \cdot (2n)!} C_{2n} e^{(2n)}(t) \cos(\phi_{2n} - \phi_d) \\
& + \frac{1}{2(2n+1)!} C_{2n+1} e^{(2n+1)}(t) \sin(\phi_{2n+1} - \phi_d) + \dots \dots \dots
\end{aligned} \tag{3.40}$$

This is the response of the carrier-modulated systems. The Laplace transform of this equation takes the next form

$$M(s) = G(s) E(s) \tag{3.41}$$

from which the transfer function of this system is obtained. The transfer function of the carrier-modulated system is then

$$\begin{aligned}
G(s) = & \frac{1}{2} C_0 \cos(\phi_0 - \phi_d) + \frac{1}{2} C_1 s \sin(\phi_1 - \phi_d) + \frac{1}{2 \cdot 2!} C_2 s^2 \cos(\phi_2 - \phi_d) \\
& + \frac{1}{2 \cdot 3!} C_3 s^3 \sin(\phi_3 - \phi_d) + \dots \dots \dots + \frac{1}{2 \cdot (2n)!} C_{2n} s^{2n} \cos(\phi_{2n} - \phi_d) \\
& + \frac{1}{2 \cdot (2n+1)!} C_{2n+1} s^{2n+1} \sin(\phi_{2n+1} - \phi_d) + \dots \dots \dots
\end{aligned} \tag{3.42}$$

Let  $\phi_d = 0$  as a particular case the transfer function reduces to

$$\begin{aligned}
G_1(s) = & \frac{1}{2} \left\{ C_0 \cos \phi_0 + C_1 s \sin \phi_1 + \frac{1}{2!} C_2 s^2 \cos \phi_2 \right. \\
& + \frac{1}{3!} C_3 s^3 \sin \phi_3 + \dots \dots \dots + \frac{1}{(2n)!} C_{2n} s^{2n} \cos \phi_{2n} \\
& \left. + \frac{1}{(2n+1)!} C_{2n+1} s^{2n+1} \sin \phi_{2n+1} + \dots \dots \dots \right\}
\end{aligned} \tag{3.43}$$

Using the following relations which are derived from eq.(3.35)

$$\left. \begin{aligned} C_{2n} \cos \phi_{2n} &= M^{(2n)}(j\omega_0) \\ C_{2n+1} \sin \phi_{2n+1} &= N^{(2n+1)}(j\omega_0) \end{aligned} \right\} \tag{3.44}$$

the transfer function of eq.(3.43) is simplified as

$$\begin{aligned}
G_1(s) = & \frac{1}{2} \left\{ M(j\omega_0) + s N'(j\omega_0) + \frac{1}{2!} s^2 M''(j\omega_0) + \frac{1}{3!} s^3 N^{(3)}(j\omega_0) \right. \\
& + \dots \dots \dots + \frac{1}{(2n)!} s^{2n} M^{(2n)}(j\omega_0) + \frac{1}{(2n+1)!} s^{2n+1} N^{(2n+1)}(j\omega_0) \\
& \left. + \dots \dots \dots \right\}
\end{aligned} \tag{3.45}$$

when  $\phi_d = \pi/2$  as a next example the transfer function is

$$\begin{aligned}
G_2(s) = & \frac{j}{2} \left\{ N(j\omega_0) + \frac{1}{1!} s M'(j\omega_0) + \frac{1}{2!} s^2 N''(j\omega_0) + \dots \dots \dots \right. \\
& \left. + \frac{1}{(2n)!} s^{2n} N^{(2n)}(j\omega_0) + \frac{1}{(2n+1)!} s^{2n+1} M^{(2n+1)}(j\omega_0) + \dots \dots \dots \right\}
\end{aligned} \tag{3.46}$$

The general transfer function of ac servomechanisms of eq.(3.42) is written in terms of these two transfer functions  $G_1(s)$  and  $G_2(s)$  as

$$G(s) = G_1(s) \cos \phi_d + G_2(s) \sin \phi_d \tag{3.47}$$

Usually  $\phi_d$  is taken equal to  $\phi_0$  to maximize static gain. In this case the transfer function is

$$G(s) = G_1(s) \cos \phi_0 + G_2(s) \sin \phi_0. \quad (3.48)$$

### 3.3.3 Example of Calculation

The transfer functions of carrier - modulated systems consisting of typical ac networks are calculated by the method described so far.

EX. 3.1

$$H(s) = \frac{1}{s} \quad (3.49)$$

In this case

$$M(s) = 0$$

and

$$\left. \begin{aligned} jN^{(2n)}(j\omega_0) &= (-1)^n \frac{(2n)!}{(\omega_0)^{2n+1}} \\ N^{(2n+1)}(j\omega_0) &= -(-1)^n \frac{(2n+1)!}{(\omega_0)^{2n+2}} \end{aligned} \right\} \quad (3.50)$$

By eq.(3.45) and eq.(3.46)

$$\begin{aligned} G_1(s) &= \frac{s}{\omega_0} \frac{1}{2} \left\{ \frac{1}{\omega_0} - \frac{s^2}{\omega_0^3} + \frac{s^4}{\omega_0^5} - \dots \right\} \\ G_2(s) &= \frac{1}{2} \left\{ \frac{1}{\omega_0} - \frac{s^2}{\omega_0^3} + \frac{s^4}{\omega_0^5} - \dots \right\} \\ \text{and} \\ G_1(s) &= \left\{ \frac{s}{\omega_0} \cos \phi_d + \sin \phi_d \right\} G_2(s) \end{aligned} \quad (3.51)$$

As will be easily noticed  $G_2(s)$  is written in the following analytic form.

$$G_2(s) = \frac{1}{2\omega_0} \frac{1}{1 + \left(\frac{s}{\omega_0}\right)^2} \quad (3.52)$$

The phase of demodulation signal  $\phi_d$  considerably affects the property of the transfer function. When  $\phi_d$  is zero  $G(s)$  has the property of the phase - lead network, while when  $\phi_d$  is  $\pi/2$  it has the property of the phase - lag network.

EX. 3.2

As a next example a unit lag is considered.

$$H(s) = \frac{1}{\lambda + \frac{s}{\omega_0}} \quad (3.53)$$

By differentiation we obtain

$$H^{(2n)}(s) = \left(\frac{-1}{\omega_0}\right)^n \frac{1}{\left(\lambda + \frac{s}{\omega_0}\right)^{n+1}} \quad (3.54)$$

and

$$\begin{aligned} H^{(n)}(j\omega_0) &= M^{(n)}(j\omega_0) + N^{(n)}(j\omega_0) \\ &= -\omega_0 \left\{ \left(\frac{\rho}{\omega_0}\right)^{n+1} \cos(n+1)\mu + j\left(\frac{\rho}{\omega_0}\right)^{n+1} \sin(n+1)\mu \right\} \end{aligned} \quad (3.55)$$

where

$$\left. \begin{aligned} \rho &= \frac{1}{\sqrt{1 + \lambda^2}} \\ \mu &= \pi - \tan^{-1} \frac{1}{\lambda} \end{aligned} \right\} \quad (3.56)$$

From these equations we obtain

$$\begin{aligned} G_1(s) &= -\frac{\omega_0}{2} \left\{ \frac{\rho}{\omega_0} \cos \mu + s \left(\frac{\rho}{\omega_0}\right)^2 \cos 2\mu + \frac{s^2}{2!} \left(\frac{\rho}{\omega_0}\right)^3 \cos 3\mu + \dots \right. \\ &\quad \left. + \frac{s^n}{n!} \left(\frac{\rho}{\omega_0}\right)^{n+1} \cos(n+1)\mu + \dots \right\} \end{aligned} \quad (3.57)$$

$$\begin{aligned} G_2(s) &= \frac{\omega_0}{2} \left\{ \frac{\rho}{\omega_0} \sin \mu + s \left(\frac{\rho}{\omega_0}\right)^2 \sin 2\mu + \frac{s^2}{2!} \left(\frac{\rho}{\omega_0}\right)^3 \sin 3\mu + \dots \right. \\ &\quad \left. + \frac{s^n}{n!} \left(\frac{\rho}{\omega_0}\right)^{n+1} \sin(n+1)\mu + \dots \right\} \end{aligned} \quad (3.58)$$



### EX. 3.3 Bridged T circuit

The bridged T and the twin T circuits are commonly used as phase compensation network in ac servomechanisms. The transfer functions of these circuits are derived by the method described in this chapter.

The dc transfer function of the bridged T circuit of Fig. 3.10 is as follows.

$$H(s) = \frac{1 + \left(\frac{s}{\omega_0}\right) + \left(\frac{s}{\omega_0}\right)^2}{1 + 3\left(\frac{s}{\omega_0}\right) + \left(\frac{s}{\omega_0}\right)^2} \quad (3.59)$$

which is expanded into partial fractions as

$$H(s) = 1 + \frac{2\lambda_1}{\lambda_2 - \lambda_1} \frac{1}{\frac{s}{\omega_0} + \lambda_1} - \frac{2\lambda_2}{\lambda_2 - \lambda_1} \frac{1}{\frac{s}{\omega_0} + \lambda_2} \quad (3.60)$$

where

$$\begin{aligned} \omega_0 &= 1/RC \\ \lambda_1 &= \frac{1}{2}(3 + \sqrt{5}) \\ \lambda_2 &= \frac{1}{2}(3 - \sqrt{5}) \end{aligned}$$

Denoting

$$\frac{-1}{\lambda_1 + j} = \rho_1 e^{j\mu_1} \quad \frac{-1}{\lambda_2 + j} = \rho_2 e^{j\mu_2} \quad (3.61)$$

and referring the result of the previous section lead to the transfer functions of

this system as follow.

$$\begin{aligned} G_1(s) &= \frac{1}{2} - \left( \frac{\lambda_1 \rho_1}{\lambda_2 - \lambda_1} \cos \mu_1 - \frac{\lambda_2 \rho_2}{\lambda_2 - \lambda_1} \cos \mu_2 \right) \\ &\quad - \frac{1}{\omega_0} \left( \frac{\lambda_1 \rho_1^2}{\lambda_2 - \lambda_1} \cos 2\mu_1 - \frac{\lambda_2 \rho_2^2}{\lambda_2 - \lambda_1} \cos 2\mu_2 \right) s + \dots \\ &= 0.17 + 0.224 \left( \frac{s}{\omega_0} \right) - 0.16 \left( \frac{s}{\omega_0} \right)^2 - 0.0112 \left( \frac{s}{\omega_0} \right)^3 + \dots \end{aligned} \quad (3.62)$$

$$\begin{aligned} G_2(s) &= \left( \frac{\lambda_1 \rho_1}{\lambda_2 - \lambda_1} \sin \mu_1 - \frac{\lambda_2 \rho_2}{\lambda_2 - \lambda_1} \sin \mu_2 \right) \\ &\quad + \frac{1}{\omega_0} \left( \frac{\lambda_1 \rho_1^2}{\lambda_2 - \lambda_1} \sin 2\mu_1 - \frac{\lambda_2 \rho_2^2}{\lambda_2 - \lambda_1} \sin 2\mu_2 \right) s \\ &\quad + \dots \\ &= -0.138 \left( \frac{s}{\omega_0} \right)^2 + \dots \end{aligned} \quad (3.63)$$

By inspecting the coefficients of  $s/\omega_0$  in both transfer functions the phase leading property of the bridged T circuit is obvious.

### EX. 3.4

The twin T circuit of Fig. 3.11 is also a common compensation circuit in ac servo systems. The dc transfer function of this circuit is given by

$$H(s) = \frac{1 + \left(\frac{s}{\omega_0}\right)^2}{1 + 4\left(\frac{s}{\omega_0}\right) + \left(\frac{s}{\omega_0}\right)^2} \quad (3.64)$$

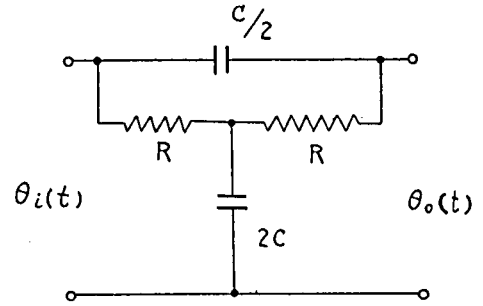


Fig. 3.10 Bridged-T compensating circuit.

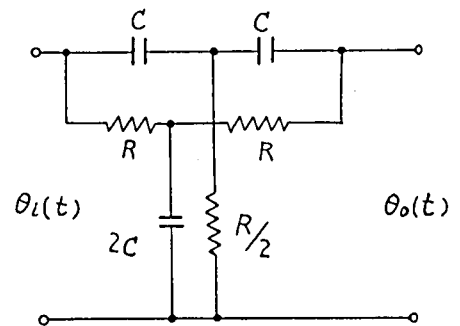


Fig. 3.11 Twin-T compensating circuit.

where,  $\omega_o = 1/RC$

$H(s)$  is expanded into following partial fractions.

$$H(s) = 1 + \frac{4\lambda_1}{\lambda_2 - \lambda_1} \cdot \frac{1}{\frac{s}{\omega_o} + \lambda_1} - \frac{4\lambda_2}{\lambda_2 - \lambda_1} \cdot \frac{1}{\frac{s}{\omega_o} + \lambda_2} \quad (3.68)$$

where

$$\begin{aligned} \lambda_1 &= 2 + \sqrt{3} \\ \lambda_2 &= 2 - \sqrt{3} \end{aligned}$$

By carrying out the similar calculations to those of EX. 3.3 the transfer functions are obtained as

$$G_1(s) = 0.223 \left(\frac{s}{\omega_o}\right) - 0.111 \left(\frac{s}{\omega_o}\right)^2 - 0.063 \left(\frac{s}{\omega_o}\right)^3 + \dots \quad (3.69)$$

$$G_2(s) = -0.0743 \left(\frac{s}{\omega_o}\right)^2 + \dots \quad (3.70)$$

It is not at all difficult to calculate coefficients to higher orders of  $s$ , but, since angular frequency of interest is always less than  $\omega_o$ , the first few terms are sufficient to understand the dynamic properties of the carrier modulated systems.

### 3.3.4 Concluding Remark

The transfer function of the carrier - modulated system has been understood from a vague analogy to the relation of transfer function to frequency response. From the result obtained in this chapter the frequency response approach to the carrier modulated system by D. Morris is justified, while the theory considering the envelope of the modulated signal is not supported.

For instance considering the transfer function of ac servoamplifier of Fig. 3.9 concerning the input signal of the chopper circuit to the output of the amplifier<sup>46)</sup> is not adequate. If this is the case,  $\theta_i(t)$  and  $\theta_o(t)$  subject to a sinusoidal signal of  $e(t)$  are

$$\begin{aligned} \theta_i(t) &= E_o \sin \omega t \cdot \cos \omega_o t \\ &= \frac{1}{2} E_o \{ \sin (\omega_o + \omega) t - \sin (\omega_o - \omega) t \} \end{aligned}$$

$$\text{and} \quad \theta_o(t) = \frac{1}{2} E_o \left[ H_1 \sin \{ (\omega_o + \omega) t + \phi_1 \} - H_2 \sin \{ (\omega_o - \omega) t + \phi_2 \} \right] \quad (3.71)$$

$$\text{If} \quad H_1 = H_2 = H \quad (3.72)$$

$$\text{then} \quad \theta_o(t) = H E_o \sin \left( \omega t + \frac{\phi_1 - \phi_2}{2} \right) \cos \left( \omega_o t + \frac{\phi_1 - \phi_2}{2} \right) \quad (3.73)$$

and the envelope  $H E_o \sin \left( \omega t + \frac{\phi_1 - \phi_2}{2} \right)$  is clearly defined. But in many cases the relation of eq.(3.73) does not hold and the envelope is even undefined.

In fact eq.(3.45) and eq.(3.46) are written in the next forms referring (3.32)

$$\begin{aligned} \text{and (3.33)} \quad G_1(s) &= \frac{1}{2} R_o \left\{ H(j\omega_o) + sH'(j\omega_o) + \frac{1}{2!} s^2 H''(j\omega_o) + \dots \right. \\ &\quad \left. + \frac{1}{(2n)!} s^{2n} H^{(2n)}(j\omega_o) + \frac{1}{(2n+1)!} s^{2n+1} H^{(2n+1)}(j\omega_o) + \dots \right\} \\ &= \frac{1}{2} R_o \{ H(j\omega_o + s) \} \\ &= \frac{1}{4} \{ H(s + j\omega_o) + H(s - j\omega_o) \} \quad (3.74) \end{aligned}$$

$$\begin{aligned}
G_2(s) &= -\frac{1}{2} I_m \left\{ H(j\omega_0) + sH'(j\omega_0) + \frac{1}{2!} s^2 H''(j\omega_0) + \dots \right. \\
&\quad \left. + \frac{1}{(2n)!} s^{2n} H^{(2n)}(j\omega_0) + \frac{1}{(2n+1)!} s^{2n+1} H^{(2n+1)}(j\omega_0) + \dots \right\} \\
&= -\frac{1}{2} I_m \{ H(j\omega_0 + s) \} \\
&= \frac{1}{4} \{ H(s + j\omega_0) - H(s - j\omega_0) \} \quad (3.75)
\end{aligned}$$

in which  $s$  is considered real number. By putting  $s = j\omega$  eq.(3.74) and eq.(3.75)

reduce to the frequency response obtained by D. Morris.

### 3.4 Transfer Function of Chopper - Modulated Circuits<sup>48) 49) 50)</sup>

#### 3.4.1 Introduction

Small ac servomechanisms including computing servomechanisms, automatic balancing instruments, X Y recorders and fire control equipments unexceptionally use choppers in the input circuit of the servoamplifier. To understand the dynamic behavior of these ac servomechanisms it is necessary to know the transfer functions of the elements constructing them. Among them the dynamic property of the chopper - modulated circuit has not been wholly understood.

As the chopper - modulated circuit is a periodically interrupted electrical network and is not describable by a simple ordinary differential equation of constant coefficients the transfer function of this circuit is not obtainable by a conventional method.

The reason that the dynamics of the chopper - modulated circuits have begun to attract the interests of electronic engineers may be attributed to the recent development of the analog computer. The author has been trying to improve the dynamic performance of the servo multiplier and began studying the transfer function of the chopper modulated circuits. The study of the transfer function of the chopper - modulated circuits is extremely important as this circuit is the only part of the servomechanisms to be investigated for improving the response of the whole system.

Several studies on this problem are recently published<sup>51) 52) 53) 54) 57) 58) 59)</sup> by which the author was very much encouraged. In those papers the dynamics of the chopper circuit are discussed in terms of the frequency response. As this is less straight forward the author has attacked the problem from the time function; that is, by calculating the transient response of the chopper - modulated circuit subject to arbitrary input signal and taking its Laplace transform<sup>p</sup> after some approximation. Although it is not readily determined as to which way of approach is superior, the frequency response approach is preferable for complex circuit

while the time function approach is more suitable to study the dc gain and the effect of the circuit constants to the transfer function of the less complex chopper - modulated circuit.

### 3.4.2 Transient Response of a Simple Chopper - Modulated circuit.

The input circuit of a simple chopper amplifier is shown in Fig. 3.12. The mechanical contact  $S$  interrupts the signal applied through  $r$  at the modulation frequency  $f_0$ . The input signal  $f(t)$  is converted into ac voltage, the waveform of which is calculated in the following way.

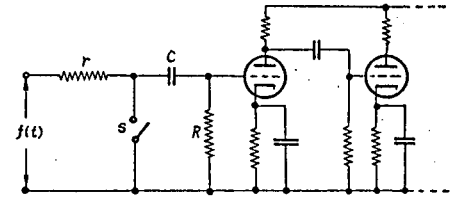


Fig. 3.12 Input circuit of a simple chopper - amplifier.

Let the duration while  $S$  is open be  $\Delta_1$  seconds and that while  $S$  is close be  $\Delta_2$  seconds, then the period of the interruption of the chopper is

$$\Delta = 1/f_0 = \Delta_1 + \Delta_2 \quad \text{seconds} \quad (3.76)$$

The circuits when  $S$  is open and when  $S$  is close are shown in Fig. 3.13 (a) and Fig. 3.13 (b) respectively.

The circuit equations for each circuit are as follows. For the circuit when  $S$  is open

$$v + (R + r) i = f(t)$$

$$C \frac{dv}{dt} = i$$

$$Ri = e$$

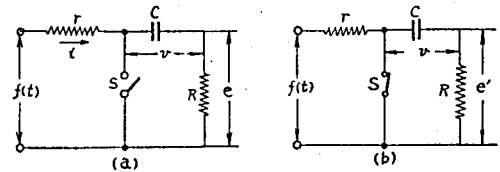


Fig. 3.13 simple chopper-modulated circuit

(3.77)

For the circuit when  $S$  is close

$$C \frac{dv'}{dt} = i'$$

$$Ri' = e'$$

(3.78)

where  $v$ ,  $e$  and  $i$  are the voltages across  $C$  and  $R$  and the current in  $R$  when  $S$  is open and  $v'$ ,  $e'$  and  $i'$  are those when  $S$  is close.

The waveform of the input signal  $f(t)$  is approximated by a staircase function as shown in Fig. 3.14, which takes constant value for the time interval of  $\Delta$  and does a sudden change at the moment of interruption of the chopper. Under this approximation the solutions of the above circuit equations are obtained as

$$e = \frac{1}{k} (f_n - v_0) e^{-\frac{t-n\Delta}{k\tau}}, \quad \text{for } n\Delta < t \leq n\Delta + \Delta_1 \quad (3.79)$$

$$e' = -v_0' e^{-\frac{t-n\Delta-\Delta_1}{\tau}}, \quad \text{for } n\Delta + \Delta_1 < t \leq (n+1)\Delta \quad (3.80)$$

where

$$k = 1 + r/R$$

$$r = RC$$

(3.81)

The waveform of this chopper circuit is alike one shown in Fig. 3.15. Denoting the voltage across R at the moment immediately before the contact S closes at the  $n$ th interruption period by  $e_n$  and that at the moment immediately before S opens by  $e_n'$  the initial values  $v_0$  and  $v_0'$  in the above solutions are written as

$$v_0 = -e_{n-1} - 1 \quad (3.82)$$

$$v_0' = f_n - ke_n \quad (3.83)$$

according to the fact that the electric charge of the capacitance is unchanged at the moment of the interruption of the circuit unless infinite current is allowed.

Substituting eq.(3.82) into eq.(3.79) and let  $t = n\Delta + \Delta_1$ , we obtain

$$e_n = \frac{1}{k} (f_n + e_{n-1}') e^{-\frac{\Delta_1}{k\tau}} \quad (3.84)$$

Similarly, substituting eq.(3.83) into eq.(3.80) and let  $t = (n+1)\Delta$ , we obtain

$$e_n' = (ke_n - f_n) e^{-\frac{\Delta_2}{\tau}} \quad (3.85)$$

These two equations make a non-homogeneous simultaneous difference equation which may be reduced to the following equations.

$$e_n - \lambda e_{n-1} = \frac{1}{k} e^{-\frac{\Delta_1}{k\tau}} (f_n - e^{-\frac{\Delta_2}{\tau}} f_{n-1}) \quad (3.86)$$

$$e_n' - \lambda e_{n-1}' = -e^{-\frac{\Delta_2}{\tau}} (1 - e^{-\frac{\Delta_1}{k\tau}}) f_n \quad (3.87)$$

where

$$\lambda = e^{-\frac{1}{\tau}(\frac{\Delta_1}{k} + \Delta_2)} \quad (3.88)$$

The solution of the nonhomogeneous difference equation is obtainable by the following method.  $e_n$ ,  $e_n'$  and  $f_n$  are considered staircase function of  $t$  which take constant values for the time interval of  $\Delta$  as shown in Fig. 3.16; that is

$$\left. \begin{aligned} e(t) &= e_n, & n\Delta < t \leq (n+1)\Delta \\ e'(t) &= e_n', & " \\ f(t) &= f_n, & " \end{aligned} \right\} \quad (3.89)$$

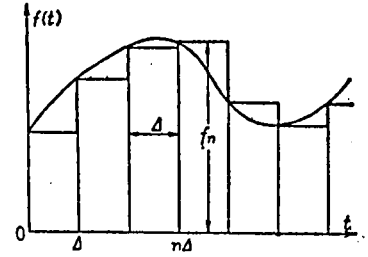


Fig. 3.14 Approximating inputs signal by staircase function

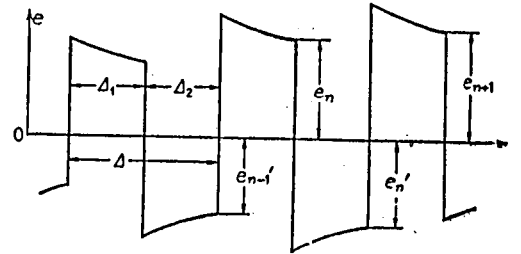


Fig. 3.15 Output waveform of the chopper-modulated circuit.

By definition they have the following property

$$\left. \begin{aligned} e(t - \Delta) &= e_{n-1} \\ e'(t - \Delta) &= e'_{n-1} \\ f(t - \Delta) &= f_{n-1} \end{aligned} \right\} \quad (3.90)$$

and we can take the Laplace transform of these

staircase functions. Let

$$\mathcal{L}[e(t)] = E(s), \mathcal{L}[e'(t)] = E'(s), \mathcal{L}[f(t)] = F(s)$$

then

$$\left. \begin{aligned} \mathcal{L}[e(t - \Delta)] &= e^{-s\Delta} E(s) = Z^{-1} E(s) \\ \mathcal{L}[e'(t - \Delta)] &= Z^{-1} E'(s) \\ \mathcal{L}[f(t - \Delta)] &= Z^{-1} F(s) \end{aligned} \right\} \quad (3.91)$$

where

$$Z = e^{s\Delta} \quad (3.92)$$

is the shift operater.

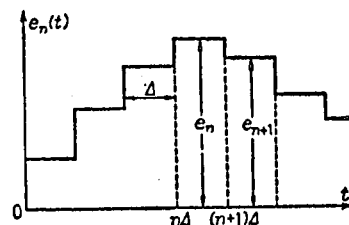


Fig. 3.16 Considering solution of difference equation as staircase function of time.

Now the difference equations of eq.(3.86) and eq.(3.87) are Laplace - transformed into the following equations.

$$E(s) - \lambda Z^{-1} E(s) = \frac{1}{k} e^{-\frac{\Delta_1}{k\tau}} \left\{ F(s) - e^{-\frac{\Delta_2}{\tau}} Z^{-1} F(s) \right\} \quad (3.93)$$

$$E(s) - \lambda Z^{-1} E'(s) = -e^{-\frac{\Delta_2}{\tau}} (1 - e^{-\frac{\Delta_1}{k\tau}}) F(s) \quad (3.94)$$

Solving these equations for  $E(s)$  and  $E'(s)$  the transfer functions for these variables

are derived as

$$G_1(s) = \frac{E(s)}{F(s)} = \frac{e^{-\frac{\Delta_1}{k\tau}}}{k} \frac{1 - e^{-\frac{\Delta_2}{\tau}} Z^{-1}}{1 - \lambda Z^{-1}} \quad (3.95)$$

$$G_2(s) = \frac{E'(s)}{F(s)} = \frac{-e^{-\frac{\Delta_2}{\tau}} (1 - e^{-\frac{\Delta_1}{k\tau}})}{1 - \lambda Z^{-1}} \quad (3.96)$$

In this result we see the output voltage of the chopper - modulated circuit has different transfer functions as to when S is open or close. This fact had been unrevealed until T. Numakura experimentally verified.<sup>54) 56)</sup> He used an assumption to explain the phenomenon which was not supported by the theory. The result obtained above clearly explained the experiment by T. Numakura.

The transient response of the chopper - modulated circuit is obtainable by expanding  $G_1(s)$  and  $G_2(s)$  into infinite series of  $Z^{-1}$  like

$$G_1(s) = \frac{e^{-\frac{\Delta_1}{k\tau}}}{k} \left\{ 1 - e^{-\frac{\Delta_2}{\tau}} (1 - e^{-\frac{\Delta_1}{k\tau}}) (Z^{-1} + \lambda Z^{-2} + \lambda^2 Z^{-3} + \dots) \right\} \quad (3.97)$$

$$G_2(s) = -e^{-\frac{\Delta_2}{\tau}} (1 - e^{-\frac{\Delta_1}{k\tau}}) (1 + \lambda Z^{-1} + \lambda^2 Z^{-2} + \dots) \quad (3.98)$$

$$\text{Using the relation } \mathcal{L}\left[\frac{Z^{-n}}{s}\right] = H(t - n\Delta) \quad (3.99)$$

where  $H(t)$  denotes unit function the step responses are obtained as

$$e_n = \frac{1}{k} e^{-\frac{\Delta_1}{k\tau}} \left\{ 1 - e^{-\frac{\Delta_2}{\tau}} (1 - e^{-\frac{\Delta_1}{k\tau}}) \sum_{i=0}^{n-1} \lambda^i \right\} \quad (3.100)$$

$$e_n' = -e^{-\frac{\Delta_2}{\tau}} (1 - e^{-\frac{\Delta_1}{k\tau}}) \cdot \sum_{i=0}^n \lambda^i \quad (3.101)$$

which are shown in Fig. 3.17. This result agrees to the result obtained by Okazaki.<sup>55)</sup>

The frequency response of the chopper - modulated circuit is also derived from the

transfer function by putting  $s = j\omega$  in  $G_1(s)$  and  $G_2(s)$ . They are

$$|G_1(j\omega)| = \frac{e^{-\frac{\Delta_1}{k\tau}}}{k} \sqrt{\frac{1 - 2e^{-\frac{\Delta_2}{\tau}} \cos \omega\Delta + e^{-\frac{\Delta_2}{\tau}}}{1 - 2\lambda \cos \omega\Delta + \lambda^2}} \quad (3.102)$$

$$\angle G_1(j\omega) = \tan^{-1} \frac{e^{-\frac{\Delta_2}{\tau}} \sin \omega\Delta}{1 - e^{-\frac{\Delta_2}{\tau}} \cos \omega\Delta} - \tan^{-1} \frac{\lambda \sin \omega\Delta}{1 - \lambda \cos \omega\Delta} \quad (3.103)$$

$$|G_2(j\omega)| = \frac{e^{-\frac{\Delta_2}{\tau}} (1 - e^{-\frac{\Delta_1}{k\tau}})}{\sqrt{1 - 2\lambda \cos \omega\Delta + \lambda^2}} \quad (3.104)$$

$$\angle G_2(j\omega) = \tan^{-1} \frac{\lambda \sin \omega\Delta}{1 - \lambda \cos \omega\Delta} \quad (3.105)$$

The frequency responses calculated from the above equations are plotted in Fig. 3.18. The experimental results are also shown in this figure, which considerably agree to the theoretical curves.

The Lissajous' figures observed when measuring the frequency response of the chopper-modulated circuit are shown in Fig. 3.19. In these figures thin ellipses declining to the right correspond to  $e(t)$  and the thick ellipses declining to the left to  $e'(t)$ . The different character of the frequency responses of  $e(t)$  and  $e'(t)$  is clearly observable from these figures.

From the frequency response plots of Fig. 3.18 the phase-leading property of  $G_1(s)$  may be observed. As the matter of fact for lower frequencies  $G_1(s)$  and  $G_2(s)$  are approximately written

$$G_1(s) \cong \frac{e^{-\frac{\Delta_1}{k\tau}} \lambda}{k(1-\lambda)} \cdot \frac{1 + \frac{\Delta e^{-\frac{\Delta_2}{\tau}}}{1 - e^{-\frac{\Delta_2}{\tau}}} \cdot s}{1 + \frac{\lambda\Delta}{1-\lambda} \cdot s} = K_1 \cdot \frac{1 + \alpha T_0 s}{1 + T_0 s} \quad (3.106)$$

$$G_2(s) \cong \frac{e^{-\frac{\Delta_2}{\tau}} \cdot \lambda}{1 - \lambda} \cdot \frac{1}{1 + \frac{\lambda\Delta}{1-\lambda} \cdot s} = \frac{-K_2}{1 + T_0 s} \quad (3.107)$$

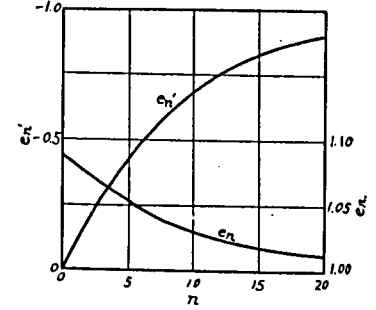


Fig. 3.17 Step response of the chopper-modulated circuit of Fig. 3.13.

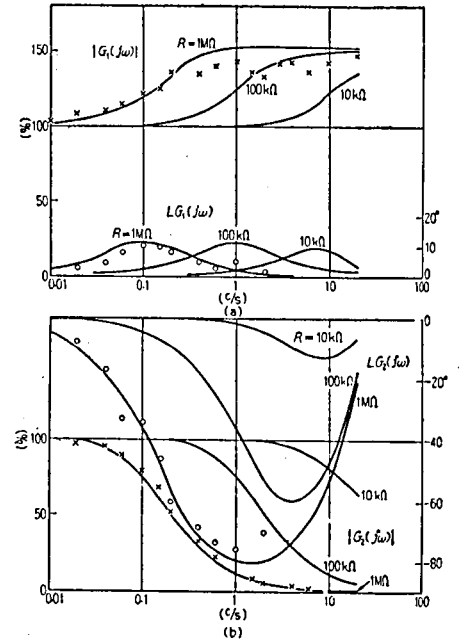
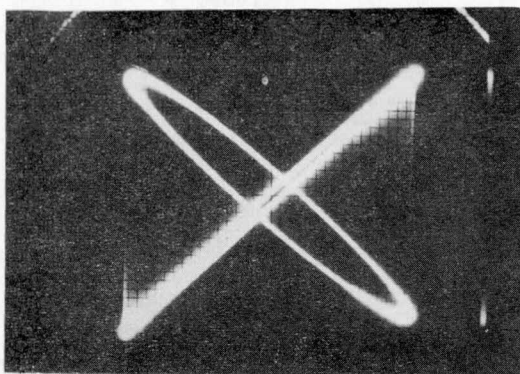
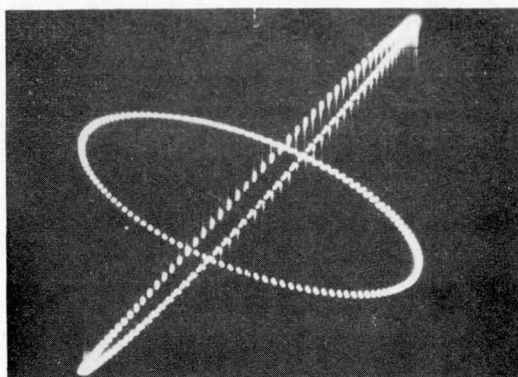


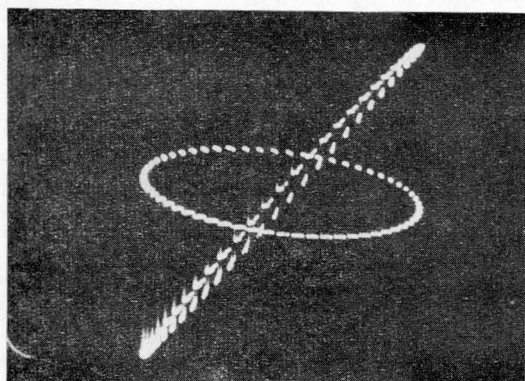
Fig. 3.18 Frequency response of the chopper-modulated circuit of Fig. 3.13. Solid lines are calculated response and crosses and dots are experimental results.



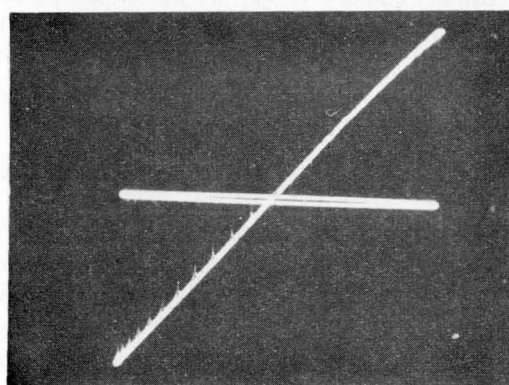
(a)  $f = 0.08 \text{ c/s}$



(b)  $f = 0.4 \text{ c/s}$



(c)  $f = 0.8 \text{ c/s}$



(d)  $f = 15 \text{ c/s}$

Fig. 3.19 Lissajon's figures of a Chopper - modulated circuit.



by using the following approximation

$$Z^{-1} \approx 1 - s\Delta \quad (3.108)$$

$T_o$ , the time constant appearing in these approximate transfer functions may be considered the response time of the chopper - modulated circuit, which is

$$T_o = \frac{\lambda \Delta}{1 - \lambda} = \frac{\Delta e^{-\left(\frac{\Delta_1}{k\tau} + \Delta_2\right)}}{1 - e^{-\left(\frac{\Delta_1}{k\tau} + \Delta_2\right)}} \quad (3.109)$$

The dependence of  $T_o$  on the time constant of the circuit  $RC = \tau$  is described in Fig. 3.20 in which it is taken that  $\Delta_1 = \Delta_2 = \Delta/2$ . Usually  $\tau$  is larger than  $\Delta$  so that the approximate formula

$$T_o \approx \frac{2k}{k+1} \cdot \tau \quad (3.110)$$

satisfies many cases. This is a useful formula as it gives general idea on the response time of the chopper - modulated circuit  $\alpha$ , the index of the phase - lead in eq.(3.106) is given by

$$\alpha = \frac{1}{e^{-\frac{\Delta_1}{k\tau}} - e^{-\left(\frac{\Delta_1}{k\tau} + \frac{\Delta_2}{\tau}\right)}} \quad (3.111)$$

The dependence of  $\alpha$  on  $\tau$  is shown in Fig. 3.21

when  $\Delta_1 = \Delta_2 = \frac{\Delta}{2}$ . The following approximation again holds when  $\tau$  is larger than  $\Delta$ .

$$\alpha \approx \frac{k+1}{k} \quad (3.112)$$

The balanced - type chopper - modulated circuit of Fig. 3.22 is often used.

The transfer function of this circuit is  $G_1(s) G_2(s)$  as the output of this circuit is  $e - e'$ .

Finally the transfer functions of the chopper modulated circuit of Fig. 3.23 is derived by a similar method. They are

$$G_1(s) = e^{-\frac{\Delta_1}{\tau}} \cdot \frac{1 - e^{-\frac{\Delta_2}{k\tau}} \cdot Z^{-1}}{1 - \lambda Z^{-1}} \quad (3.113)$$

$$G_2(s) = -\frac{e^{-\frac{\Delta_2}{k\tau}}}{k} \cdot \frac{1 - e^{-\frac{\Delta_1}{\tau}} Z^{-1}}{1 - \lambda Z^{-1}} \quad (3.114)$$

which resemble the transfer function of the chopper - modulated circuit of Fig. 3.12.

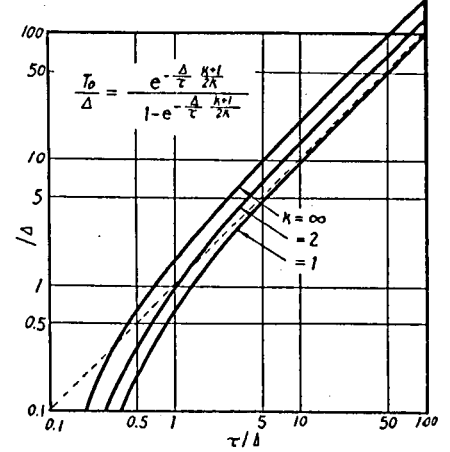


Fig. 3.20 Time constant of the chopper - modulated circuit of Fig. 3.13 as a function of the time constant of the circuit.

$$G_1(s) = e^{-\frac{\Delta_1}{\tau}} \cdot \frac{1}{1 - \lambda Z^{-1}} \cdot e^{-\frac{\Delta_2}{k\tau}} \quad (3.113)$$

$$G_2(s) = e^{-\frac{\Delta_1}{k\tau}} \cdot \frac{1}{k} \cdot \frac{1}{1 - \lambda Z^{-1}} \cdot e^{-\frac{\Delta_2}{\tau}} \quad (3.114)$$

### 3.4.3 Non - resonant Chopper - Modulated Circuits

Generally the chopper - modulated circuits are classified into two types, namely resonant and non - resonant chopper - modulated circuits.

The chopper - modulated circuit consisting of the capacitors and resistors described in the previous section are of non - resonant type, while the circuit using an input transformer tuned by a capacitor at the frequency of the interruption of chopper belongs to the resonant type. The waveform of the output of the circuit of both types are shown in Fig. 3.24. The difference between the waveforms of the resonant and non - resonant chopper - modulated circuit is that the former changes oscillatory while the latter changes monotonically during the interruption period. From this reason different methods of calculating the response of the chopper circuits have to be used depending the type of the circuit. In this section the transfer function of general non - resonant chopper - modulated circuit is studied.

Consider a contact  $S$  interrupting a branch of an electrical network consisting  $m$  capacitors and inductances and a certain number of resistances. A signal  $f(t)$  is applied to this network as an input. Let  $\Delta_1$  represent the period during which  $S$  is close and  $u_1, u_2, \dots, u_m$  denote the voltage drops of the capacitances and the currents of the inductances while  $S$  is close. The period during which  $S$  is

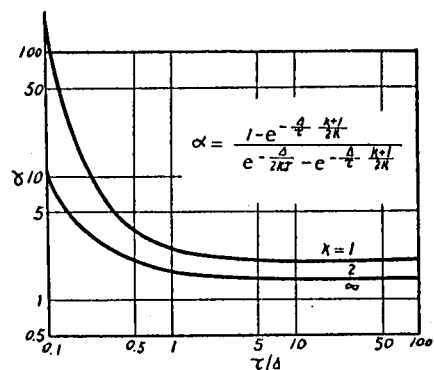


Fig. 3.21 Index of phase - lead of the chopper - modulated circuit of Fig. 3.13 as a function of circuit time constant

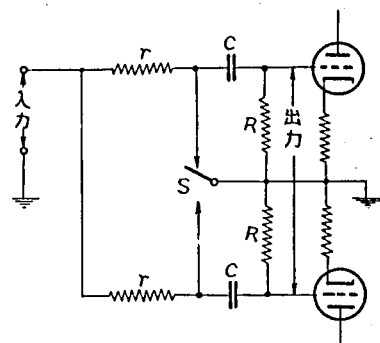


Fig. 3.22 Double ended chopper - modulated circuit.

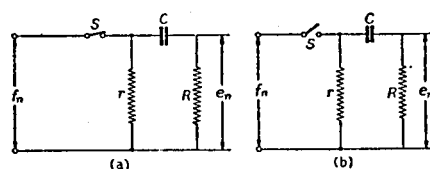


Fig. 3.23 A simple chopper - modulated circuit.

open is written as  $\Delta_2$  and the voltage drops of the capacitances and the currents of the inductances when S is open are denoted  $u_1'$ ,  $u_2'$ , ...,  $u_m'$  as well.

As the terminal voltages of the capacitances and the currents in the inductances are conserved at the instant of the interruption of the switch unless infinite current or infinite voltage is allowed (which is unusual case) the initial values of these voltages and currents used for solving the circuit equation at each interruption

period are those values at the moment immediately before the transition of the switch.

The solution of the circuit equation when S is open is given in the following equation. In solving the circuit equation  $f(t)$  is replaced by a staircase function as that of Fig. 3.14.

$$\begin{pmatrix} u_1 \\ u_2 \\ \vdots \\ u_m \end{pmatrix} = \begin{pmatrix} \alpha_{11}(f) & \alpha_{12}(f) & \dots & \alpha_{1m}(f) \\ \alpha_{21}(f) & \alpha_{22}(f) & \dots & \alpha_{2m}(f) \\ \vdots & \vdots & \ddots & \vdots \\ \alpha_{m1}(f) & \alpha_{m2}(f) & \dots & \alpha_{mm}(f) \end{pmatrix} \begin{pmatrix} u_{10} \\ u_{20} \\ \vdots \\ u_{m0} \end{pmatrix} + f_m \begin{pmatrix} \alpha_1(t) \\ \alpha_2(t) \\ \vdots \\ \alpha_m(t) \end{pmatrix} \quad (3.115)$$

where  $\alpha_i(t)$  is the indicial response of  $u$  to the input signal when initial values of  $u_1, u_2, \dots, u_m$  are zero,  $\alpha_{ij}(t)$  is the solution of  $u_i$  when input signal and initial values of all  $u$ 's except that of  $u_j$  are zero and the initial value of  $u_j$  is unity, and  $u_{10}, u_{20}, \dots, u_{m0}$  are the initial values of  $u_1, u_2, \dots, u_m$  which are the values of  $u_1', u_2', \dots, u_m'$  immediately before the contact S opens. The origin of time in the above equation is taken at the moment of transition of the switch, when we denote

$$\left. \begin{aligned} \alpha_{ij}(\Delta_1) &= \alpha_{ij} \\ \alpha_i(\Delta_1) &= \alpha_i \end{aligned} \right\} \quad (3.116)$$

the values of  $u_1, u_2, \dots, u_m$  at  $t = \Delta_1$ ,  $u_{1n}, u_{1n'}, u_{2n}, \dots, u_{mn}$  are obtained from eq.(3.115) as

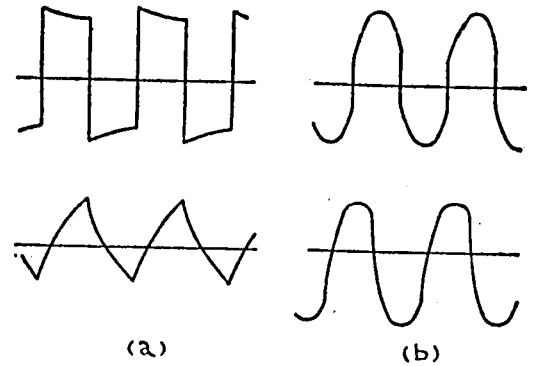


Fig. 3.24 Output waveforms of chopper - modulated circuits,  
(a) non - resonant circuit.  
(b) resonant circuit.

$$\begin{pmatrix} u_{1n} \\ u_{2n} \\ \vdots \\ u_{mn} \end{pmatrix} = \begin{pmatrix} \alpha_{11} & \alpha_{12} & \dots & \alpha_{1m} \\ \alpha_{21} & \alpha_{22} & \dots & \alpha_{2m} \\ \vdots & \vdots & \ddots & \vdots \\ \alpha_{m1} & \alpha_{m2} & \dots & \alpha_{mm} \end{pmatrix} \begin{pmatrix} u'_{1, n-1} \\ u'_{2, n-1} \\ \vdots \\ u'_{m, n-1} \end{pmatrix} + f_n \begin{pmatrix} \alpha_1 \\ \alpha_2 \\ \vdots \\ \alpha_m \end{pmatrix} \quad (3.117)$$

where  $u'_{in}$  is the value of  $u_i'$  at the end of  $n$ th interruption period.

Likewise  $U_{in}'$  are represented in terms of  $u_{in}$  as follow.

$$\begin{pmatrix} u'_{1n} \\ u'_{2n} \\ \vdots \\ u'_{mn} \end{pmatrix} = \begin{pmatrix} \beta_{11} & \beta_{12} & \dots & \beta_{1m} \\ \beta_{21} & \beta_{22} & \dots & \beta_{2m} \\ \vdots & \vdots & \ddots & \vdots \\ \beta_{m1} & \beta_{m2} & \dots & \beta_{mm} \end{pmatrix} \begin{pmatrix} u_{1n} \\ u_{2n} \\ \vdots \\ u_{mn} \end{pmatrix} + f_n \begin{pmatrix} \beta_1 \\ \beta_2 \\ \vdots \\ \beta_m \end{pmatrix} \quad (3.118)$$

where  $\beta_{ij}$  and  $\beta_i$  have similar meaning to  $\alpha_{ij}$  and  $\alpha_i$ .

Now  $u_1, u_2, \dots, u_m$  etc. are represented by vectors, and  $(\alpha_{ij})$  etc. are represented by matrices as follow.

$$\begin{pmatrix} u_{1n} \\ u_{2n} \\ \vdots \\ u_{mn} \end{pmatrix} = \vec{u}_n, \quad \begin{pmatrix} u'_{1n} \\ u'_{2n} \\ \vdots \\ u'_{mn} \end{pmatrix} = \vec{u}'_n$$

$$\begin{pmatrix} \alpha_1 \\ \alpha_2 \\ \vdots \\ \alpha_m \end{pmatrix} = \vec{\alpha}, \quad \begin{pmatrix} \beta_1 \\ \beta_2 \\ \vdots \\ \beta_m \end{pmatrix} = \vec{\beta}$$

$$(\alpha_{ij}) = A, \quad (\beta_{ij}) = B$$

Using these expressions eq.(3.117) and eq.(3.118) are rewritten as

$$\vec{u}_n = A \cdot \vec{u}'_{n-1} + f_n \cdot \vec{\alpha} \quad (3.119)$$

$$\vec{u}'_n = B \cdot \vec{u}_n + f_n \cdot \vec{\beta} \quad (3.120)$$

from which the following difference equations are obtained.

$$\vec{u}_n - A \cdot B \cdot \vec{u}_{n-1} = f_n \cdot \alpha + A \cdot \vec{\beta} \quad (3.121)$$

$$\vec{u}'_n - B \cdot A \cdot \vec{u}'_{n-1} = f_n (B \cdot \alpha + \vec{\beta}) \quad (3.122)$$

$\vec{u}_n$  and  $\vec{u}'_n$  are now assumed staircase functions taking constant values for an

interval of  $\Delta$  ( $= \Delta_1 + \Delta_2$ ) and their Laplace transforms are written  $\vec{U}(s)$  and  $\vec{U}'(s)$ .

Then, by taking the Laplace transform of the difference equations of eq.(3.121) and

eq.(3.122) the transfer functions of the non - resonant chopper - modulated circuit are

obtained. They are

$$\vec{G}_1(s) = \frac{\vec{U}(s)}{F(s)} = [E - Z^{-1} \cdot A \cdot B]^{-1} \cdot (\alpha + Z^{-1} A \cdot \vec{\beta}) \quad (3.123)$$

$$\vec{G}_2(s) = \frac{\vec{U}'(s)}{F(s)} = [E - Z^{-1} \cdot B \cdot A]^{-1} \cdot (B \cdot \alpha + \vec{\beta}) \quad (3.124)$$

where E denotes unit matrix.

For the single ended chopper - modulated circuit the amplitude of the output signal is  $(u + u') / 2$ . The transfer function is then

$$G(s) = \frac{1}{2} (G_1(s) + G_2(s)) \quad (3.125)$$

In general the output voltage of the chopper - modulated circuit is represented by a

linear combination of  $u_{is}'$  and  $u_{is}''$ , that is

$$\left. \begin{aligned} E &= \sum C_i u_i = \vec{C}' \cdot \vec{u} \\ E' &= \sum C'_i u'_i = \vec{C}'' \cdot \vec{u}' \end{aligned} \right\} \quad (3.126)$$

The transfer functions of this circuit are then

$$\left. \begin{aligned} H_1(s) &= \vec{C}' \cdot \vec{G}_1(s) \\ H_2(s) &= \vec{C}'' \cdot \vec{G}_2(s) \end{aligned} \right\} \quad (3.127)$$

Thus we have derived a general form of the transfer functions of the non - resonant chopper - modulated circuit. The calculation of A, B,  $\vec{\alpha}$  and  $\vec{\beta}$  is not easy in practical cases. Although they are readily obtainable in the forms of P function what we need are t functions. The use of the analog computer is highly recommended.

#### 3.4.4 Resonant Chopper - Modulated Circuits.

The resonant chopper - modulated circuit using input transformer and tuning capacitor such as is shown in Fig. 3.25 has a certain amount of gain and also produces a sinusoidal waveform. The output signal of the resonant chopper - modulated circuit is as shown in Fig. 3.23 (b) and the amplitude of the waveform is no longer represented by the magnitude at the transition of the switch as was done for the non - resonant circuit. It was decided, therefore, to represent the amplitude of the modulated wave by the magnitude of the signal at the middle of the interruption period. When Q value

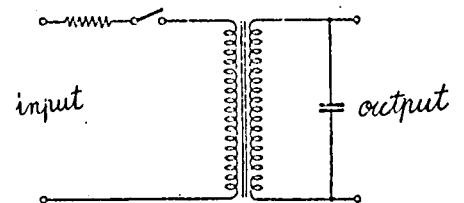
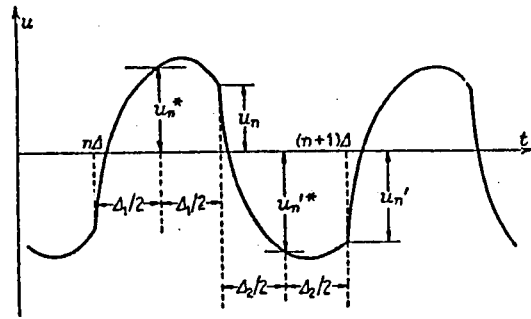


Fig. 3.25 A resonant chopper - modulated circuit.

of the circuit is sufficiently large the output waveform is nearly sinusoidal and this approximation holds good.

As shown in Fig. 3.26 the magnitudes of the voltages of the capacitances and the currents of inductances of the resonant chopper - modulated circuit when the contact is close and when it is open are denoted by  $\vec{u}_n^*$  and  $\vec{u}_n'^*$  respectively. Then



following equations are obtained by a similar procedure to that described in the previous section.

Fig. 3.26 Output waveform of the resonant chopper - modulated circuit.

$$\vec{u}_n^* = A^* \cdot \vec{u}_{n-1} + f_n \cdot \vec{\alpha}^* \quad (3.128)$$

$$\vec{u}_n'^* = B^* \cdot \vec{u}_n + f_n \cdot \vec{\beta}^* \quad (3.129)$$

where

$$\left. \begin{aligned} A^* &= (\alpha_{ij}^*) = \left\{ \alpha_{ij} \left( \frac{\Delta_1}{2} \right) \right\} \\ (\alpha_i^*) &= \left\{ \alpha_i \left( \frac{\Delta_1}{2} \right) \right\} \\ B^* &= (\beta_{ij}^*) = \left\{ \beta_{ij} \left( \frac{\Delta_2}{2} \right) \right\} \\ (\beta_i^*) &= \left\{ \beta_i \left( \frac{\Delta_2}{2} \right) \right\} \end{aligned} \right\} \quad (3.130)$$

The transfer functions of  $\vec{u}^*$  and  $\vec{u}'^*$  are then written in terms of  $G_1(s)$  and  $G_2(s)$  of eq.(3.123) and eq.(3.124) which are the transfer functions of  $\vec{u}$  and  $\vec{u}'$ , as

$$\vec{G}_1^*(s) = Z^{-1} \cdot A^* \cdot \vec{G}_2(s) + \vec{\alpha}^* \quad (3.131)$$

$$\vec{G}_2^*(s) = B^* \cdot \vec{G}_1(s) + \vec{\beta}^* \quad (3.132)$$

These are the general forms of the transfer functions of the resonant chopper - modulated circuit.

As an example the transfer function of the unbalanced resonant chopper - modulated circuit of Fig. 3.25 is calculated. The equivalent circuit is shown in Fig. 3.27. The circuit equations are

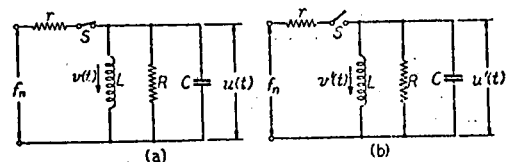


Fig. 3.27 Equivalent circuit of the chopper - modulated circuit of Fig. 3.25.

$$C \frac{du}{dt} = \frac{1}{r} (f_n - u) - \frac{u}{R} - v \quad (3.133)$$

$$L \frac{dv}{dt} = u \quad (3.134)$$

$$C \frac{du'}{dt} = -\frac{u'}{R} - v' \quad (3.135)$$

$$L \frac{dv'}{dt} = u' \quad (3.136)$$

where  $u$  and  $u'$  are the voltage - drops of the capacitance and  $v$  and  $v'$  are the currents in the inductance. Eq.(3.133) and eq.(3.134) are now Laplace transformed considering initial values of  $u$ ,  $v$ ,  $u'$  and  $v'$ , resulting

$$U(s) = \frac{LCs^2 \cdot u_0 + \frac{L}{r} sf_n - Lv_0}{LCs^2 + L(\frac{1}{R} + \frac{1}{r})s + 1} \quad (3.137)$$

$$V(s) = \frac{\{LCs^2 + L(\frac{1}{R} + \frac{1}{r})s\} v_0 + Csu_0 + \frac{1}{r} f_n}{LCs^2 + L(\frac{1}{R} + \frac{1}{r})s + 1} \quad (3.138)$$

By taking the inverse Laplace transforms of  $U(s)$  and  $V(s)$  following members of the matrices of eq.(3.130) are obtained.

$$\alpha_{11}(t) = e^{-\frac{k\omega_0 t}{2Q}} \left( \cos \sqrt{1 - \frac{k^2}{4Q^2}} \omega_0 t - \frac{\frac{k}{2Q}}{\sqrt{1 - \frac{k^2}{4Q^2}}} \sin \sqrt{1 - \frac{k^2}{4Q^2}} \omega_0 t \right) \quad (3.139)$$

$$\alpha_{12}(t) = -\frac{\omega_0 L}{\sqrt{1 - \frac{k^2}{4Q^2}}} e^{-\frac{k\omega_0 t}{2Q}} \sin \sqrt{1 - \frac{k^2}{4Q^2}} \omega_0 t \quad (3.140)$$

$$\alpha_{21}(t) = \frac{\frac{1}{\omega_0 L}}{\sqrt{1 - \frac{k^2}{4Q^2}}} e^{-\frac{k\omega_0 t}{2Q}} \sin \sqrt{1 - \frac{k^2}{4Q^2}} \omega_0 t \quad (3.141)$$

$$\alpha_{22}(t) = e^{-\frac{k\omega_0 t}{2Q}} \left( \cos \sqrt{1 - \frac{k^2}{4Q^2}} \omega_0 t + \frac{\frac{k}{2Q}}{\sqrt{1 - \frac{k^2}{4Q^2}}} \sin \sqrt{1 - \frac{k^2}{4Q^2}} \omega_0 t \right) \quad (3.142)$$

$$\alpha_1(t) = \frac{\frac{\omega_0 L}{r}}{\sqrt{1 - \frac{k^2}{4Q^2}}} e^{-\frac{k\omega_0 t}{2Q}} \sin \sqrt{1 - \frac{k^2}{4Q^2}} \omega_0 t \quad (3.143)$$

$$\alpha_2(t) = \frac{1}{r} \left\{ 1 - e^{-\frac{k\omega_0 t}{2Q}} \left( \cos \sqrt{1 - \frac{k^2}{4Q^2}} \omega_0 t + \frac{\frac{k}{2Q}}{\sqrt{1 - \frac{k^2}{4Q^2}}} \sin \sqrt{1 - \frac{k^2}{4Q^2}} \omega_0 t \right) \right\} \quad (3.144)$$

Likewise eq.(3.135) and eq.(3.136) are solved to obtain following results.

$$\beta_{11}(t) = e^{-\frac{\omega_0 t}{2Q}} \left( \cos \sqrt{1 - \frac{1}{4Q^2}} \omega_0 t - \frac{1}{\sqrt{1 - \frac{1}{4Q^2}}} \sin \sqrt{1 - \frac{1}{4Q^2}} \omega_0 t \right) \quad (3.145)$$

$$\beta_{12}(t) = -\frac{\omega_0 L}{\sqrt{1 - \frac{1}{4Q^2}}} e^{-\frac{\omega_0 t}{2Q}} \sin \sqrt{1 - \frac{1}{4Q^2}} \omega_0 t \quad (3.146)$$

$$\beta_{21}(t) = \frac{1}{\sqrt{1 - \frac{1}{4Q^2}}} e^{-\frac{\omega_0 t}{2Q}} \sin \sqrt{1 - \frac{1}{4Q^2}} \omega_0 t \quad (3.147)$$

$$\beta_{22}(t) = e^{-\frac{\omega_0 t}{2Q}} \left( \cos \sqrt{1 - \frac{1}{4Q^2}} \omega_0 t + \frac{1}{\sqrt{1 - \frac{1}{4Q^2}}} \sin \sqrt{1 - \frac{1}{4Q^2}} \omega_0 t \right) \quad (3.148)$$

$$\beta_1(t) = \beta_2(t) = 0 \quad (3.149)$$

In the above equations following notations are used.

$$\left. \begin{aligned} k &= 1 + \frac{R}{r} \\ \omega_0 &= \frac{1}{\sqrt{LC}} = \frac{2\pi}{\Delta} \\ Q &= \frac{R}{\omega_0 L} \end{aligned} \right\} \quad (3.150)$$

If  $\Delta_1 = \Delta_2 = \Delta/2$ , then

$$\omega_0 \Delta_1 = \omega_0 \Delta_2 = \pi$$

Assuming  $Q > 1$ , and  $Q/k > 1$ , and putting  $t = \Delta_1$  in eq.(3.139) - eq.(3.149) the matrices  $A$ ,  $B$ ,  $\vec{\alpha}$  and  $\vec{\beta}$  are obtained in simpler forms as

$$A = e^{-\frac{k\pi}{2Q}} \begin{pmatrix} -1 & 0 \\ 0 & -1 \end{pmatrix} \quad (3.151)$$

$$B = e^{-\frac{\pi}{2Q}} \begin{pmatrix} -1 & 0 \\ 0 & -1 \end{pmatrix} \quad (3.152)$$

$$\vec{\alpha} = \frac{1}{r} (1 + e^{-\frac{k\pi}{2Q}}) \begin{pmatrix} 0 \\ 1 \end{pmatrix} \quad (3.153)$$

$$\vec{\beta} = 0 \quad (3.154)$$

Under the same assumption  $A^*$ ,  $B^*$ ,  $\vec{\alpha}^*$  and  $\vec{\beta}^*$  are obtained as

$$A^* = \frac{1}{\sqrt{1 - \frac{k^2}{4Q^2}}} \cdot e^{-\frac{k\pi}{4Q}} \begin{pmatrix} -\frac{k}{2Q} & -\omega_0 L \\ \frac{\omega_0 L}{2Q} & \frac{k}{2Q} \end{pmatrix} \quad (3.155)$$

$$B^* = \frac{1}{\sqrt{1 - \frac{1}{4Q^2}}} \cdot e^{-\frac{\pi}{4Q}} \begin{pmatrix} -\frac{1}{2Q} & -\omega_0 L \\ \frac{\omega_0 L}{2Q} & \frac{1}{2Q} \end{pmatrix} \quad (3.156)$$

$$\vec{\alpha}^* = \left( \frac{\omega_0 L}{r} \cdot \frac{e^{-\frac{k\pi}{4Q}}}{\sqrt{1 - \frac{k^2}{4Q^2}}} \begin{pmatrix} \frac{k}{2Q} \\ \frac{1}{2Q} \end{pmatrix} \right) \quad (3.157)$$

$$\vec{\beta}^* = 0 \quad (3.158)$$



Substituting these into eq.(3.123) and eq.(3.124) and then into eq.(3.131) and eq.(3.132) leads to following results.

$$\vec{G}_1(s) = \frac{1+e^{-\frac{k\pi}{2Q}}}{r} \begin{pmatrix} 0 \\ 1 - Z^{-1} \cdot e^{-\frac{k+1}{2Q}\pi} \end{pmatrix} \quad (3.159)$$

$$\vec{G}_2(s) = -e^{-\frac{\pi}{2Q}} \vec{G}_1(s) \quad (3.160)$$

$$\vec{G}_1^*(s) = \begin{pmatrix} \frac{\omega_0 L}{r} e^{-\frac{k\pi}{4Q}} \frac{1 + Z^{-1} \cdot e^{-\frac{k}{2Q}\pi}}{1 - Z^{-1} \cdot e^{-\frac{k+1}{2Q}\pi}} \\ \frac{1}{r} \left[ 1 - \frac{k}{2Q} e^{-\frac{k\pi}{4Q}} \frac{1 + Z^{-1} \cdot e^{-\frac{\pi}{2Q}}}{1 - Z^{-1} \cdot e^{-\frac{k+1}{2Q}\pi}} \right] \end{pmatrix} \quad (3.161)$$

$$\vec{G}_2^*(s) = -\frac{\omega_0 L}{r} \cdot \frac{e^{-\frac{\pi}{4Q}} + e^{-\frac{2k+1}{4Q}\pi}}{1 - Z^{-1} \cdot e^{-\frac{k+1}{2Q}\pi}} - \frac{1}{2Qr} \cdot \frac{e^{-\frac{\pi}{4Q}} + e^{-\frac{2k+1}{4Q}\pi}}{1 - Z^{-1} \cdot e^{-\frac{k+1}{2Q}\pi}} \quad (3.162)$$

The transfer functions of the terminal voltage of the capacitor of this chopper circuit are  $G_{11}^*(s)$  and  $G_{21}^*(s)$ , which are

$$G_{11}^*(s) = K \cdot \frac{1 + \alpha \mu Z^{-1}}{1 - \mu Z^{-1}} \quad (3.163)$$

$$G_{21}^*(s) = \frac{K'}{1 - \mu Z^{-1}} \quad (3.164)$$

where

$$\left. \begin{aligned} K &= \frac{\omega_0 L}{r} e^{-\frac{k\pi}{4Q}} \\ K' &= \frac{\omega_0 L}{r} e^{-\frac{k\pi}{4Q}} \left( 1 + e^{-\frac{k\pi}{2Q}} \right) \\ \mu &= e^{-\frac{k+1}{2Q}\pi} \\ \alpha &= e^{-\frac{k\pi}{2Q}} \end{aligned} \right\} \quad (3.165)$$

The indicial response of the output voltage of this circuit is

$$u(t) = K(1 + \alpha) \sum_{i=0}^n \mu^i - k\alpha \quad (3.166)$$

$$u'(t) = K' \sum_{i=0}^n \mu^i \quad (3.167)$$

for  $n \triangleleft t \leq (n+1) \triangle$

These results were calculated for a particular case where

$$Q = 80, \quad k = 32.4$$

and are plotted in Fig. 3.28 together with the analog computer results.

The static gains of this resonant chopper - modulated circuit are also obtainable from the transfer functions of eq.(3.161) and eq.(3.162) by putting  $s = 0$ . They are

$$G_{11}^*(0) = \frac{\omega_0 L}{r} e^{-\frac{k\pi}{4Q}} \frac{1 + e^{-\frac{\pi}{2Q}}}{1 + e^{-\frac{k+1}{2Q}\pi}} \quad (3.168)$$

$$G_{21}^*(0) = -\frac{\omega_0 L}{r} e^{-\frac{\pi}{4Q}} \frac{1 + e^{-\frac{k\pi}{2Q}}}{1 - e^{-\frac{k+1}{2Q}\pi}} \quad (3.169)$$

The ratio of  $G_{11}^*(0)$  to  $G_{21}^*(0)$  is

$$\left| \frac{G_{11}^*(0)}{G_{21}^*(0)} \right| = \frac{e^{-\frac{k\pi}{4Q}} (1 + e^{-\frac{\pi}{2Q}})}{e^{-\frac{\pi}{4Q}} (1 + e^{-\frac{k\pi}{2Q}})} \quad (3.170)$$

which approaches unity as  $Q$  increases.

The equivalent time constant of this resonant chopper circuit is calculated by the similar method used for the non - resonant circuit as follows.

$$T_0 = \frac{\mu \Delta}{1 - \mu} = \frac{\Delta}{e^{\frac{k+1}{2Q}\pi} - 1} \quad (3.171)$$

In Fig. 3.29 the dependence of  $T_0/\Delta$  on  $Q$  is shown for different values of  $k$ .

As  $Q$  becomes larger the response of the circuit becomes more sluggish. When  $Q$  is large the following approximation holds.

$$\frac{T_0}{\Delta} \approx \frac{2Q}{(k+1)\pi} \quad (3.172)$$

This result was previously obtained by H. Tohma who derived the transfer function from the frequency response of the circuit.<sup>53)</sup>

Finally the frequency response of this resonant chopper circuit is calculated from eq.(3.163) and eq.(3.164) by putting  $s = j\omega$ .

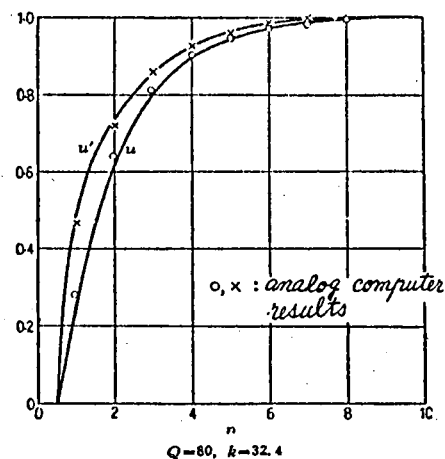


Fig. 3.28 Step response of the chopper - modulated circuit of Fig. 3.26. Solid lines are calculated response and crosses and dots are analog computer results.

$$G_{11}^*(j\omega) = K \sqrt{\frac{1 + 2\alpha\mu \cos \omega\Delta + \alpha^2 \mu^2}{1 - 2\mu \cos \omega\Delta + \mu^2}} \quad (3.173)$$

$$G_{11}^*(j\omega) = -\tan^{-1} \frac{\mu \sin \omega\Delta}{1 - \mu \cos \omega\Delta} \tan^{-1} \frac{\alpha \mu \sin \omega\Delta}{1 + \alpha \mu \cos \omega\Delta} \quad (3.174)$$

$$G_{21}^*(j\omega) = \frac{K'}{\sqrt{1 - 2\mu \cos \omega\Delta + \mu^2}} \quad (3.175)$$

$$G_{21}^*(j\omega) = -\tan^{-1} \frac{\mu \sin \omega\Delta}{1 - \mu \cos \omega\Delta} \quad (3.176)$$

The frequency response calculated from these equations are plotted in Fig. 3.30 with the results obtained by the analog computer.

As a next example the balanced type resonant chopper - modulated circuit of Fig. 3.31 is considered. In the balanced circuit it is equivalent to consider the input signal changes its sign at every  $\Delta/2$  seconds, that is, the input signal shown in Fig. 3.32 is applied to the circuit of Fig. 3.27 (a). The results of the calculation are as follow.

$$A = B = e^{-\frac{k\pi}{2Q}} \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix} \quad (3.177)$$

$$\vec{\alpha} = \vec{\beta} = \frac{1}{r} (1 + e^{-\frac{k\pi}{2Q}}) \begin{pmatrix} 0 \\ 1 \end{pmatrix} \quad (3.178)$$

$$A^* = B^* = \frac{1}{\sqrt{1 - \frac{k^2}{4Q^2}}} e^{-\frac{k\pi}{4Q}} \begin{pmatrix} -\frac{k}{2Q} & -\omega L \\ \omega L & \frac{k}{2Q} \end{pmatrix} \quad (3.179)$$

$$\vec{\alpha}^* = -\vec{\beta}^* = \begin{pmatrix} \frac{\omega L}{r} \frac{e^{-\frac{k\pi}{4Q}}}{\sqrt{1 - \frac{k^2}{4Q^2}}} \\ \frac{1}{r} \left[ 1 - \frac{2Q}{\sqrt{1 - \frac{k^2}{4Q^2}}} e^{-\frac{k\pi}{4Q}} \right] \end{pmatrix} \quad (3.180)$$

The transfer functions are obtained as.

$$\vec{G}_1^*(s) = \begin{pmatrix} \frac{\omega L}{r} \frac{e^{-\frac{k\pi}{4Q}}}{\sqrt{1 - \frac{k^2}{4Q^2}}} \left[ 1 + \frac{(1 + e^{-\frac{k\pi}{2Q}})^2 Z^{-1}}{1 - Z^{-1} e^{-\frac{k\pi}{Q}}} \right] \\ \frac{1}{r} \left[ 1 - \frac{k}{2Q} e^{-\frac{k\pi}{4Q}} \left\{ 1 + \frac{(1 + e^{-\frac{k\pi}{2Q}})^2 Z^{-1}}{1 - Z^{-1} e^{-\frac{k\pi}{Q}}} \right\} \right] \end{pmatrix} \quad (3.181)$$

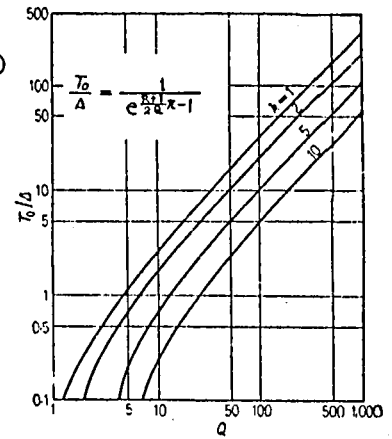


Fig. 3.29 Time constant of the chopper - modulated circuit of Fig. 3.26 as a function of  $Q$  value of the circuit.

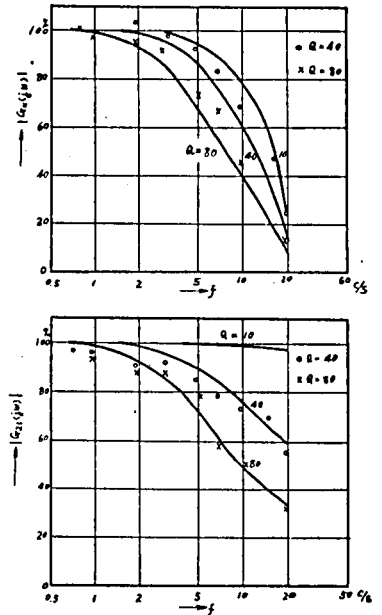


Fig. 3.30 Frequency response of the chopper modulated circuit of Fig. 3.27. Solid lines show calculated results and crosses and dots show analog computer results.

$$\vec{G}_2^*(s) = \left( \begin{array}{c} -\frac{\omega_0 L}{r} \frac{e^{-\frac{k\pi}{4Q}}}{\sqrt{1 - \frac{K^2}{4Q^2}}} \left[ 1 + \frac{(1 + e^{-\frac{k\pi}{2Q}})(1 + Z^{-1}e^{-\frac{k\pi}{2Q}})}{1 - Z^{-1}e^{-\frac{k\pi}{Q}}} \right] \\ -\frac{1}{r} \left[ 1 - \frac{\frac{k}{2Q} \cdot e^{-\frac{k\pi}{4Q}}}{\sqrt{1 - \frac{K^2}{4Q^2}}} \left\{ 1 + \frac{(1 + e^{-\frac{k\pi}{2Q}})(1 + Z^{-1}e^{-\frac{k\pi}{2Q}})}{1 - Z^{-1}e^{-\frac{k\pi}{Q}}} \right\} \right] \end{array} \right) \quad (3.182)$$

The time constant of this balanced circuit is

$$T_0 = \frac{\frac{\Delta}{k\pi}}{e^{-\frac{k\pi}{Q}} - 1} \approx \frac{\Delta Q}{k\pi} \quad (3.183)$$

which agrees with the result obtained by T. Numakura.

### 3.4.5 Analyzing the Response of the Chopper - Modulated

Circuits by the Analog Computer.

In the preceding sections the approximate formulae of the transfer function of the chopper - modulated circuits were described. In testifying the theory transient response calculated by analog computer is used rather than the experimental results obtained by actual chopper circuit. As the analysis of the transient response of the periodically interrupted electrical network by means of analog computer is of particular interests and has a wide range of applications, the outline of the way of analysis is described.

The theory of the network simulation is applied in this case, too. The block diagram of the non - resonant chopper circuit of Fig. 3.13 is shown in Fig. 3.33. As switch S interrupts the circuit periodically the circuit configuration alternates between Fig. 3.13 (a) and (b). This is also represented on the block diagram. The initial conditions are also satisfied as the outputs of the integrators  $e$ ,  $e'$ ,  $v$  and  $v'$  remain unchanged at the moment of interruption. The branch of  $r$  is the only one part of the circuit

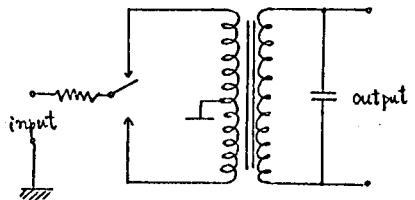


Fig. 3.31 Balanced type resonant chopper - modulated circuit.

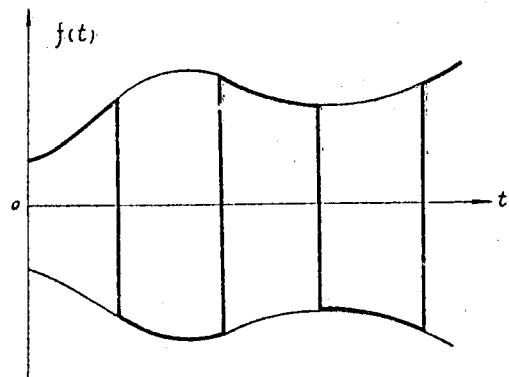


Fig. 3.32 Waveform of the equivalent input signal.

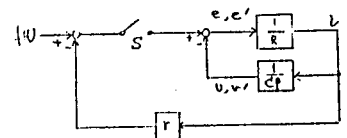


Fig. 3.33 Block diagram representation of the chopper - modulated circuit of Fig. 3.13.

not simulated during  $S$  is open, but this does not affect the voltage of the capacitor which is wanted. The analog computer circuit corresponding to the block diagram is shown in Fig.

3.34. The relay amplifier is used to operate the switch. The circuit is shown in lower part of Fig. 3.34.

The resonant chopper - modulated circuit is also analyzed on analog computer circuit.

The block diagram and the analog computer circuit of the resonant chopper circuit of Fig. 3.27 are shown in Fig. 3.35 and in Fig. 3.36 respectively.

Some of the analog computer results are shown in Fig. 3.37 and in Fig. 3.38, the former showing the response of a non - resonant chopper circuit and the latter showing the response of a resonant chopper circuit both subject to the sinusoidal input signal.

#### 3.4.6 Concluding Remark

In this part of the chapter the approximate method of calculating the transfer function of chopper - modulated circuits is presented. The basic idea of this approximate method is the use of the staircase function having the interval equal to the interruption period of the chopper. By replacing the input function  $f(t)$  by the staircase function non - homogeneous difference equations are obtained, and also by considering the variables other staircase functions of time the Laplace transforms of these difference equations are made possible. As the matter of fact this approximation admits error when the frequency of the input signal becomes comparable with the chopper frequency. Since the chopper amplifier is not supposed to transmit the signal of which frequency is comparable with that of the chopper this error is insignificant in practical cases.

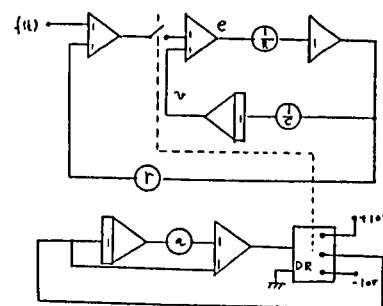


Fig. 3.34 Analog computer circuit simulating the chopper - modulated circuit Fig. 3.13.

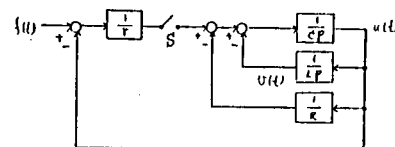


Fig. 3.35 Block diagram representation of the resonant chopper - modulated circuit of Fig. 3.27.

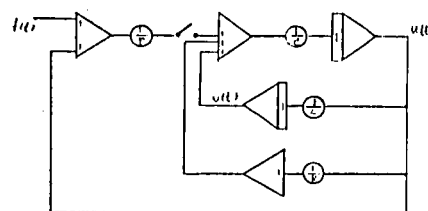


Fig. 3.36 Analog computer circuit simulating resonant chopper - modulated circuit of Fig. 3.27.

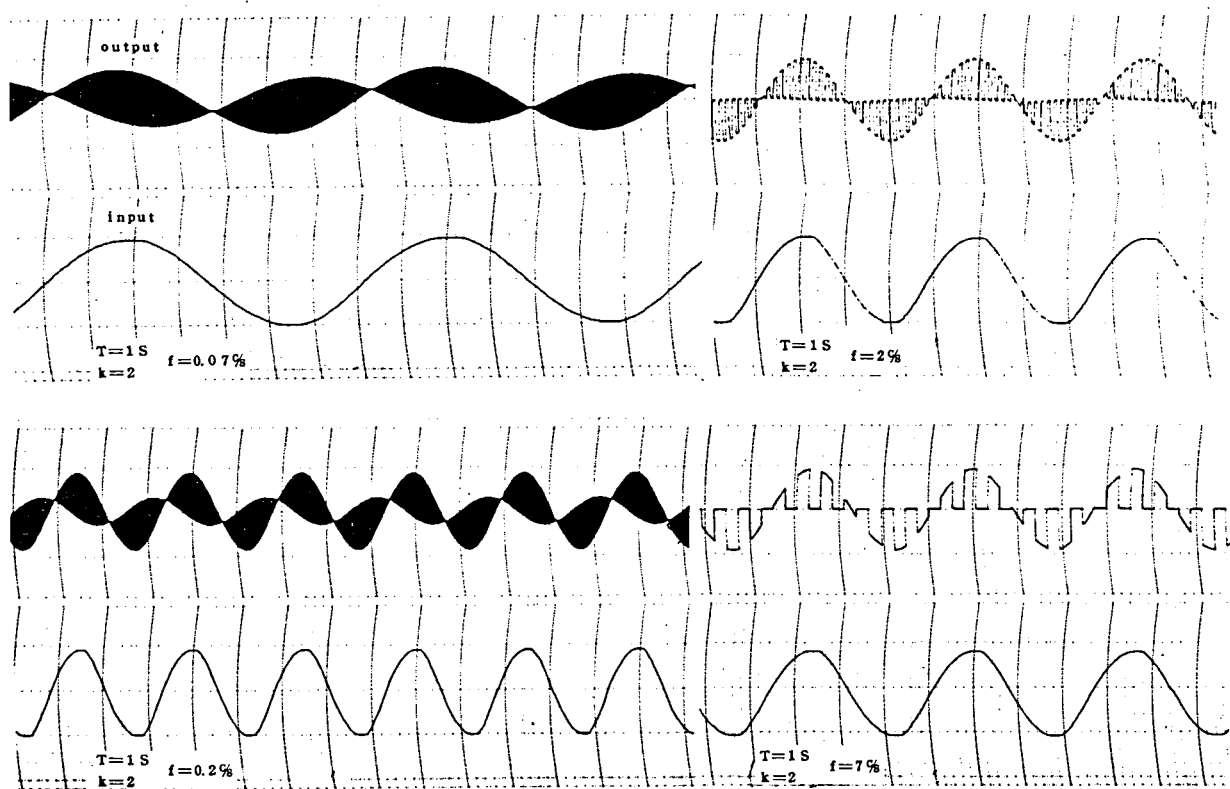


Fig. 3.37 Analog Computer Solution of Nonresonant Chopper - Circuit.

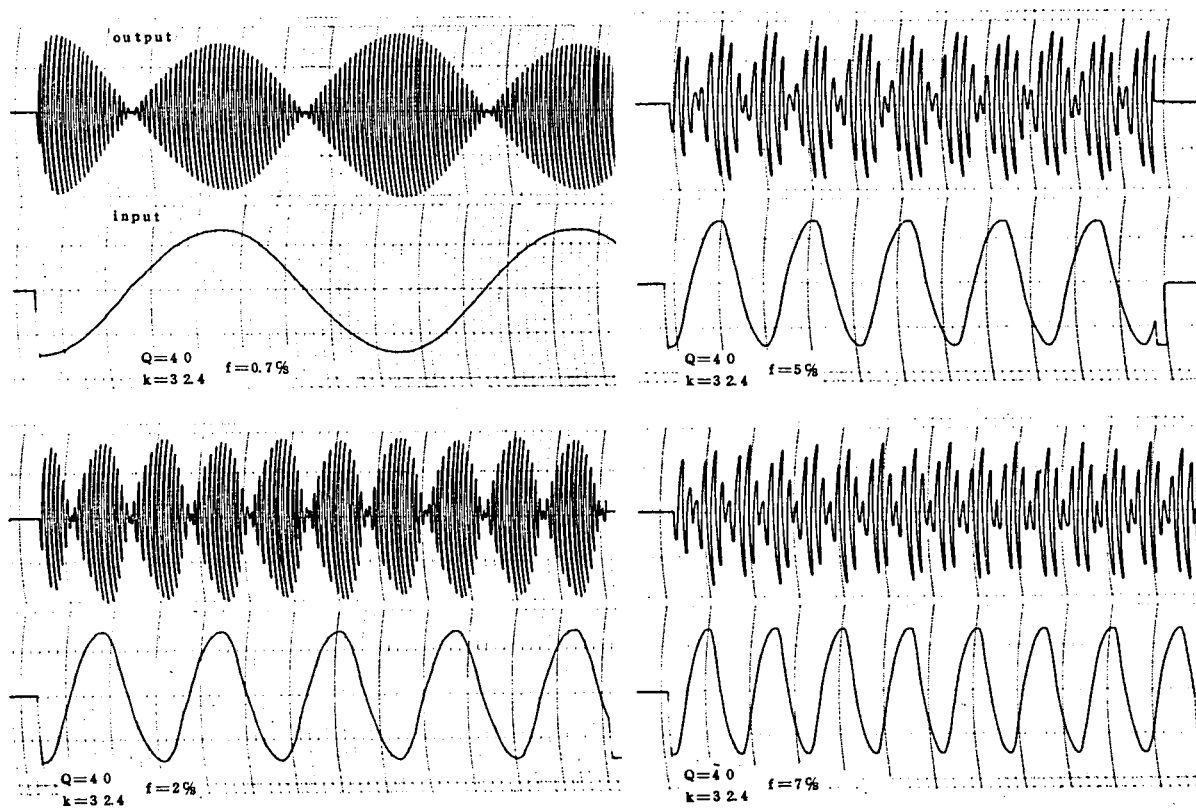


Fig. 3.38 Analog Computer Solution of Resonant Chopper Circuit.

## Chapter 4

### New Computation Techniques by Analog Computer.

#### 4. 1 Calculation of Frequency Response by Analog Computer<sup>60) 61)</sup>

Frequency response is often more conveniently used than transient response when discussing the dynamic property of a physical system. As the primary purport of the analog computer is to obtain the transient response of the physical system by solving the differential equation of the system, it has been believed that the calculation of frequency response is not suitable for analog computers. The calculation of the frequency response is, however, by no means impossible. There were a few methods for this purpose.

The first of them is to build a simulation circuit on the analog computer to which a sinusoidal signal is applied as input and to measure the amplitude and the phase of the sinusoidal output signal. The demerit of this method is that it often requires a larger bandwidth than is obtainable by the analog computer circuit.

The second method of calculating frequency response on the analog computer is the changing of the time scale factor of the analog computer circuit with the sinusoidal input signal of a constant frequency, thus changing apparent frequency of the input signal. The latter is superior to the former because of the fact that the variable frequency oscillator is unnecessary.

The third method developed by the autor is based on the transient response of the system obtainable by the analog computer.

The transfer function  $G(s)$  of a linear system is represented in the form of the frequency response  $G(j\omega)$  as

$$G(j\omega) = \int_0^{\infty} W(t) e^{-j\omega t} dt \quad (4.1)$$

where  $W(t)$  is the weighting function of the system, that is, the impulse response of the system.<sup>62)</sup> The reciprocal relation of this equation is

$$W(t) = \int_{-\infty}^{\infty} G(j\omega) e^{-j\omega t} d\omega \quad (4.2)$$

As the response of the system to the unit step input is expressed as

$$H(t) = \int_{-\infty}^{\infty} G(j\omega) \frac{e^{-j\omega t}}{j\omega} d\omega, \quad (4.3)$$

$W(t)$  is derived from  $H(t)$  as

$$W(t) = \frac{dH(t)}{dt} \quad (4.4)$$

Eq. (4.1) is then

$$G(j\omega) = \int_0^{\infty} H'(t) e^{-j\omega t} dt \quad (4.5)$$

and the real and imaginary parts of  $G(j\omega)$  are

$$P(\omega) = \int_0^{\infty} H'(t) \cos \omega t dt \quad (4.6)$$

$$Q(\omega) = -\int_0^{\infty} H'(t) \sin \omega t dt \quad (4.7)$$

Where

$$G(j\omega) = P(\omega) + j Q(\omega) \quad (4.8)$$

The author's method of frequency response calculation performs Fourier transform on the step response obtained by the analog computer according to eq. (4.6) and eq. (4.7)

The reason that eq. (4.5) instead of eq. (4.1) is used is that a unit impulse is an ideal function not obtainable by analog computer circuit while step response is most commonly obtained. In addition the differentiation is not necessary in most cases because when  $H(t)$  is the output of an integrator  $H(t)$  is present at the input of the integrator shown in Fig. 4.1.

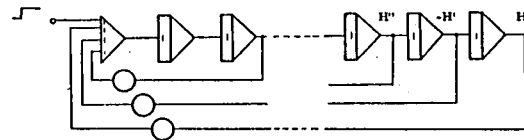


Fig. 4.1 Analog computer circuit calculating step and impulse responses.

The computations of eq. (4.6) and (4.7) are performed by the analog computer circuit of Fig. 4.2.  $H'(t)$  and  $H(t)$  are applied at two terminals of the sine - cosine potentiometer which rotates at the angular frequency of  $\omega$  rad / sec.



The time origin is taken at the instant when angle of rotation of the sine - cosine potentiometer is zero. The output signals from the sine - cosine potentiometer are then  $H'(t) \cos \omega t$  and  $H'(t) \sin \omega t$ . By in-

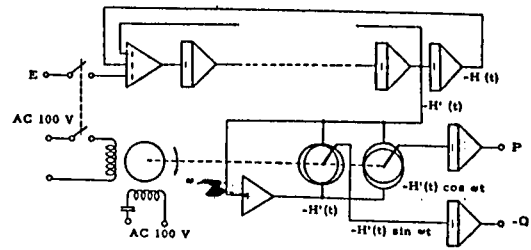


Fig. 4.2 Circuit for calculating frequency response from impulse response.

tegrating these two signals  $P(\omega)$  and

$Q(\omega)$  are obtained. Applying the obtained voltages to both terminals of a scope or of a X-Y recorder points on Nyquist's diagram are obtained for different  $\omega$ . The speed of rotation of the sine - cosine potentiometer is changed by a suitable gear train for different  $\omega$ 's. Instead of changing  $\omega$  changing the time scale of the computer circuit for generating  $H(t)$  may be feasible. The latter method is used to show an example of calculation.

Let  $t$  be the machine time as

$$t = \alpha \tau \quad (4.9)$$

Where  $\alpha$  is the time scale factor. Then

$$\int_0^{\infty} \frac{dH}{dt} e^{-j\omega \cdot t} dt = \int_0^{\infty} \frac{dH}{d\tau} e^{-j\omega \cdot \tau} d\tau \quad (4.10)$$

When we consider

$$\omega = \frac{\omega_0}{\alpha} \quad (4.11)$$

$\omega$  is changed by changing  $\alpha$ .

The transfer function measured is

$$G(s) = \frac{1}{1 + s} \quad (4.12)$$

The obtained result is shown in Fig. 4.3. The temporal changes of the output signals from the integrators are as shown in Fig. 4.4.  $P(\omega)$  and  $Q(\omega)$  are the stationary values of these signals. It should be noted that the principle of this calculation of the frequency response on the analog computer is applicable to the servo-analyzer. There is a remarkable difference between this method and the conventional method of measuring the frequency

response of a control system which measures frequency dependence of the amplitude and phase of the sinusoidal output waveform. As the latter method measures the quantities after the transient response vanishes while the author's method finishes measurement when the transient phenomenon ends, the time needed for measurement by author's method is much shorter than that by the latter. It is also noted that the conventional method needs a certain recording device of the waveform while the author's method does not. Fig. 4.5 shows the schematic diagram of the circuit for measuring the frequency response of a control system by the new method.

To conclude some problems concerning the servo-analyzer based on the new method are discussed. The most serious problems are the need of the differentiator and the use of the integrators. In the actual physical system

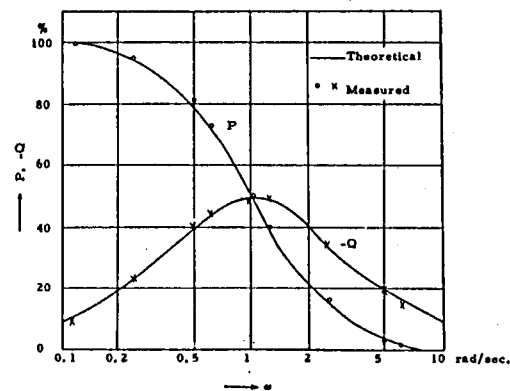


Fig. 4.3 Real part and imaginary part of the frequency response of simple transfer function :  $G(s) = \frac{1}{1+s}$   
Solid lines show theoretical and crosses and dots experimental

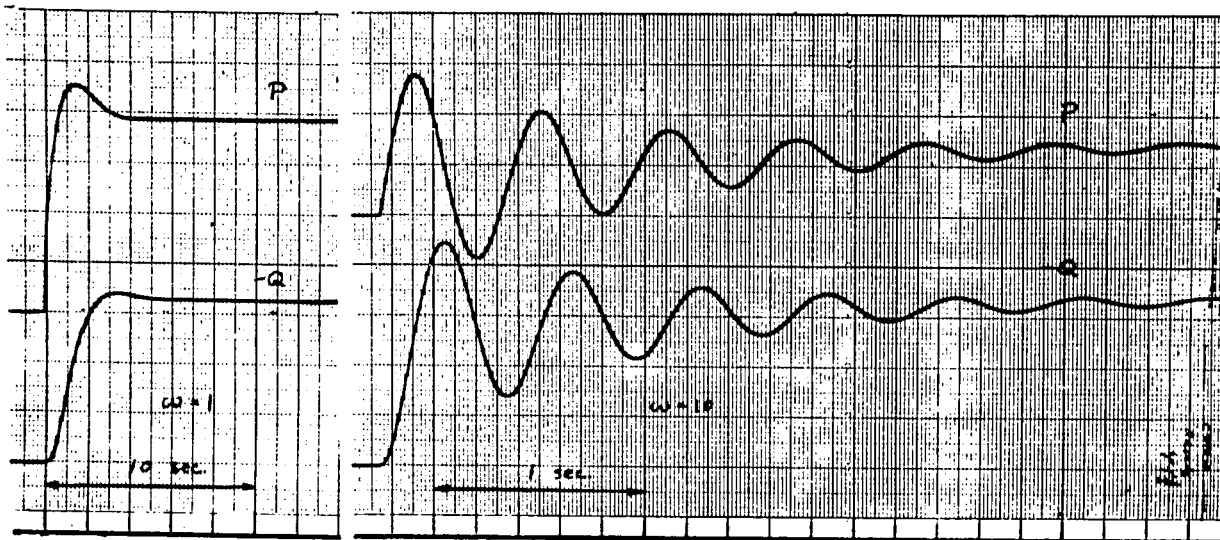


Fig. 4.4 Temporal changes of the outputs of the integrators of Fig. 4.2.

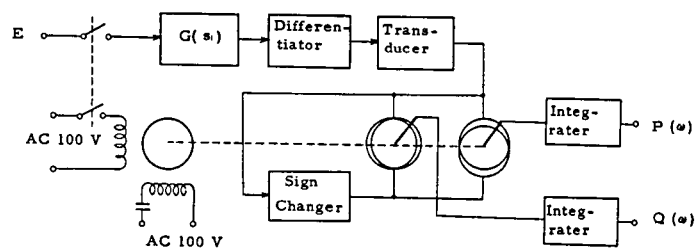


Fig. 4.5 Circuit for measuring transfer function.

considerable noise is present in the signal which, on differentiation, is amplified and deteriorates accuracy of the measurement. When the response of the system under measurement is slow integration time is long, and well balanced, drift-free integrators are needed.

Obviously the application of the new method is limited to linear systems. For systems containing nonlinear elements the transfer function obtained by the new method does not have any meaning, while the frequency response obtained by the conventional method has, at least, a meaning by the concept of the describing function.

In practice controlling the initial phase of the sine-cosine potentiometer is fairly unimportant. Let  $\phi$  be the initial phase of the potentiometer the integrations of eq. (4.6) and eq. (4.7) change into

$$\begin{aligned} X &= \int_0^{\infty} H'(t) \cos(\omega t + \phi) dt \\ &= P(\omega) \cos \phi - Q(\omega) \sin \phi \end{aligned} \quad (4.13)$$

$$\begin{aligned} Y &= \int_0^{\infty} H'(t) \sin(\omega t + \phi) dt \\ &= P(\omega) \sin \phi + Q(\omega) \cos \phi \end{aligned} \quad (4.14)$$

$P(\omega)$  and  $Q(\omega)$  are obtained by following equations

$$P(\omega) = X \cos \phi + Y \sin \phi \quad (4.15)$$

$$Q(\omega) = -X \sin \phi + Y \cos \phi \quad (4.16)$$

which are also obtained by means of analog computer circuit of Fig. 4.6.

When only the magnitude  $\sqrt{P^2 + Q^2}$  is necessary it is directly obtainable

as

$$\sqrt{P^2 + Q^2} = \sqrt{X^2 + Y^2} \quad (4.17)$$

#### 4.2 Fault Current Estimation of Mercury Rectifier Circuit

In electric railways and chemical plants mercury rectifiers are widely used as dc power supplies. The arc-back of the mercury rectifier is one of the serious faults as it causes large fault current flow in the circuit which might destroy the electric apparatus. To prevent the fault current due to arc-back the circuit should be interrupted by a circuit breaker before the fault current grows to the current unbreakable by it. Therefore the calculation of the transient change of the fault current is important for determining the specification of the circuit breaker such as the current capacity and the speed of interruption.

The mercury rectifier circuit is a kind of the interrupted circuit of which circuit equation changes depending on the time intervals. As a way of solving this discontinuous differential equation the final value of the solution in the previous time interval may be used as an initial value in the next time interval.

This kind of calculation is cumbersome, both for hand calculation and for the analog computer calculation. To avoid this difficulty the technique of the network simulation described in Chapter 1 is applied to the mercury rectifier circuit.

A three phase mercury rectifier connected to an electrolytic tank is shown in Fig. 4.7.

The equivalent circuit is shown in Fig. 4.8 where  $e_1$ ,  $e_2$ , and  $e_3$  are three phase voltages as

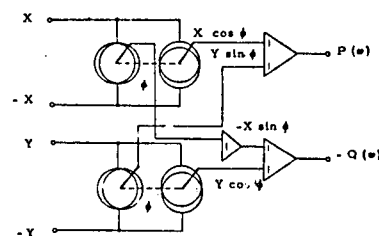


Fig. 4.6 Analog computer circuit for obtaining  $P(\omega)$  and  $Q(\omega)$  when initial angle of rotation of sine-cosine potentiometer is  $\phi$ .

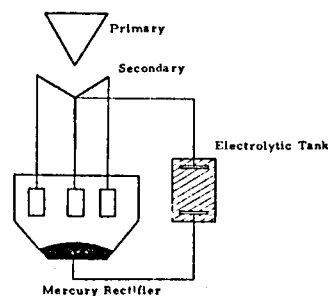


Fig. 4.7 Mercury rectifier connected to an electrolytic tank.

$$\left. \begin{aligned} e_1 &= \sqrt{2} E_o \sin \left( \omega_o t + \frac{2}{3} \pi \right) \\ e_2 &= \sqrt{2} E_o \sin \omega_o t \\ e_3 &= \sqrt{2} E_o \sin \left( \omega_o t - \frac{2}{3} \pi \right) \end{aligned} \right\} \quad (4.18)$$

In the equivalent circuit three diodes M1, M2, and M3 are used to represent the function of rectification. This is not true as the mercury rectifier is normally grid controlled. But when arc-back occurs the grids are intert and the simulation by diodes is valid for the calculation of the fault current.

The block diagram of the equivalent circuit is obtained as in Fig. 4.9.

The diodes are represented by nonlinear relation of the voltage to the current, in which the voltage drop is small for positive current and is very large for negative current. When arc-back takes

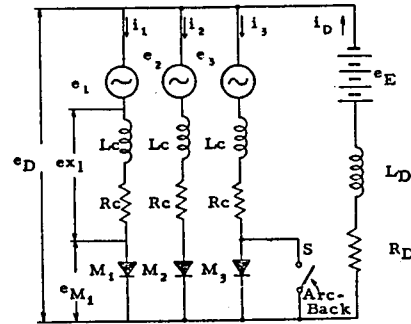


Fig. 4.8 Equivalent circuit of the mercury rectifier circuit of Fig. 4.7.

place at an anode, the function of rectification is lost in this particular anode. This phenomenon corresponds to the short circuit of diode M in the equivalent circuit, or to closing the switch S in the block diagram.

The diode characteristic is simulated by an operational amplifier with a feedback resistance and a germanium diode as input impedance. As the grid of the amplifier is always kept at zero potential the diode does not conduct for positive input voltage so that  $e_o$  is almost zero. For negative input voltage the diode conducts and large output voltage appears. The three phase ac voltages are ob-

tained by the weighted sum of two sinusoidal voltages, X and Y. That is

$$\left. \begin{aligned} X &= \frac{1}{\sqrt{2}} E_o \sin \omega t \\ Y &= \frac{1}{\sqrt{2}} E_o \cos \omega t \end{aligned} \right\} \quad (4.19)$$

$$\left. \begin{aligned} e_1 &= -X + Y \\ e_2 &= 2X \\ e_3 &= -X - Y \end{aligned} \right\} \quad (4.20)$$

The calculation of the fault current starts when the switch S is closed. Observing the current of the third phase  $I_3$  after  $I_d$  reaches at the steady state S is disclosed while  $I_3$  is zero. The arc-back begins when  $I_3$  begins to flow to the backward direction after S is disclosed. Examples of the calculated result are given in Fig. 4.10 showing  $I_3$  and  $I_d$ .

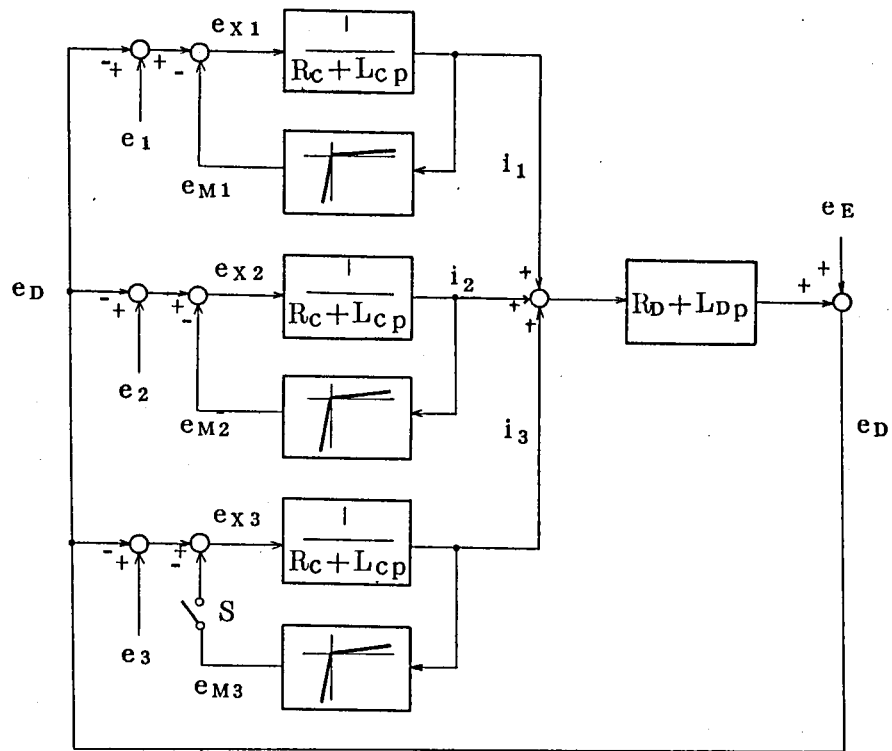


Fig. 4.9 Block diagram of the mercury rectifier circuit of Fig. 4.7

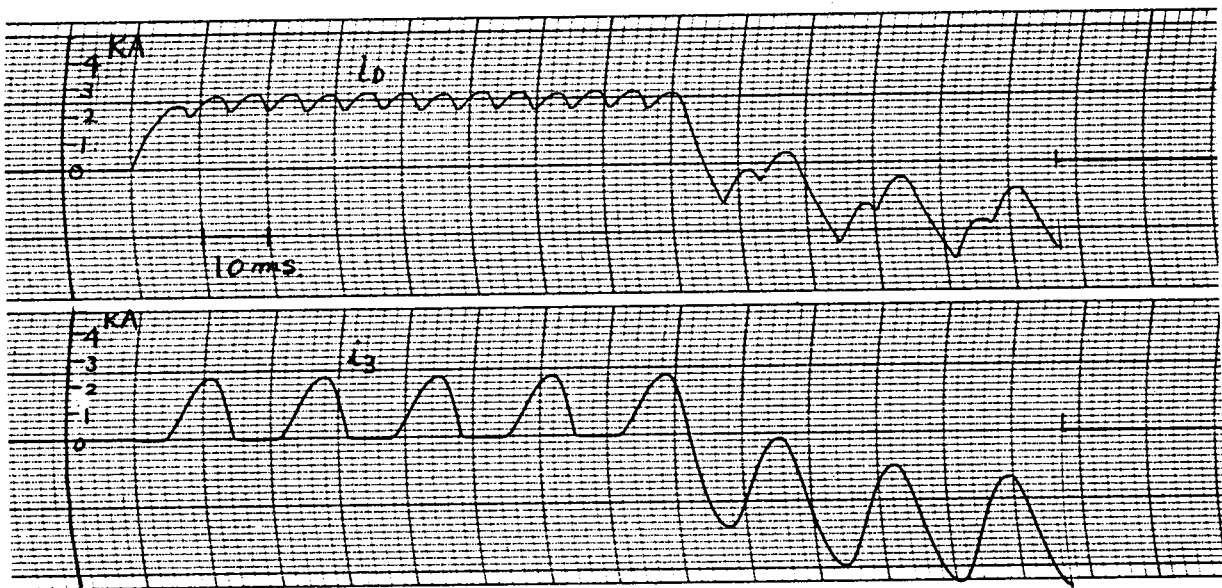


Fig. 4.10 (a) Solution of fault current of the mercury rectifier circuit with resistive load by analog computer.

$$\sqrt{2} E_o = 400 \text{ v}$$

$$e_E = 350 \text{ v}$$

$$L_c = 0.5 \text{ mH}$$

$$R_c = 0.025 \text{ ohm}$$

$$L_D = 0$$

$$R_D = 0.5 \text{ ohm}$$

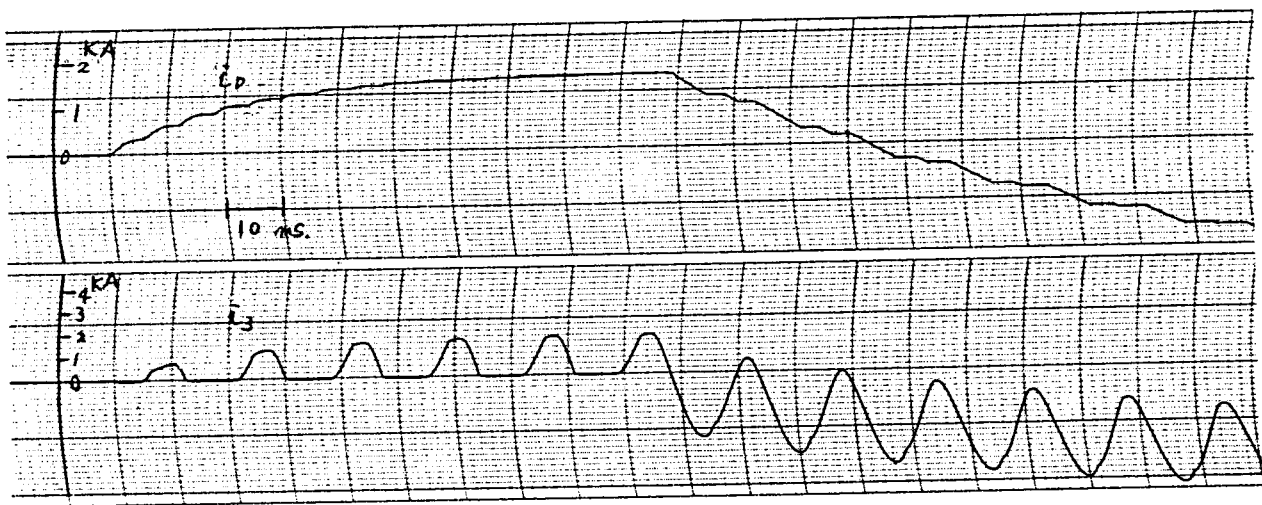


Fig. 4.10 (b) Solution of fault current of the mercury rectifier circuit with inductive load by analog computer.

$$\sqrt{2} E_o = 400 \text{ v}$$

$$e_E = 350 \text{ v}$$

$$L_c = 0.5 \text{ mH}$$

$$R_c = 0.025 \text{ ohm}$$

$$L_D = 2.0 \text{ mH}$$

$$R_D = 0$$



#### 4. 3 Automatic Programming Applied to Two-Points Boundary Value Problems 64) 65) 66)

##### 4. 3. 1 Introduction.

As the analog computer<sup>u</sup> are naturally made to solve initial value problems of differential equation it is powerless to the boundary value problems. One attempt of solving the latter problem by the analog computer is the substitution method of M. Sugano . 67) In this method the solution of a second order differential equation, for example, is written as

$$Y(t) = A(t) \cdot Y_0 + B(t) \cdot Y_0' \quad (4.21)$$

The solution of any linear homogeneous differential equation is represented by a linear combination of the initial values. The substitution method finds initial values satisfying the boundary condition by definite number of repeated trials. This method is useful for linear differential equation but is not applicable to nonlinear equations and also to the eigen value problems.

The next method of solving the boundary value problems on analog computer is the trial method in which initial values are changed step-wise for each run of the computer until the boundary condition is satisfied. The trial method is a time consuming method although it is applicable both for linear and nonlinear equations. When there are more than two boundary conditions the trial method is almost impossible as there are too many combinations of initial values to be tried.

The automatic programming of the analog computer developed by the author for two-points boundary value problems performs the trial method by the decision made by the computer itself and eliminates the demerit of the trial method.

The method of automatic programming is explained by the following example which is a second order differential equation with boundary conditions at  $t = 0$  and  $t = t_0$ .

$$y'' + 2\zeta \omega_0 y' + \omega_0^2 y = f(t) \quad (4.22)$$

$$t = 0, \quad y = 0 \quad (4.23)$$

$$t = t_0, \quad y = y_0 \quad (4.24)$$

The automatic solution of this problem is performed by the analog computer circuit of Fig. 4.11.

A part of the analog computer circuit surrounded by the dotted rectangle solves differential equation of (4.22) under the initial condition

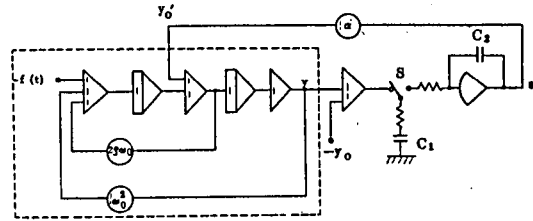


Fig. 4.11 Analog computer circuit for automatic computation of the boundary value problem of eq. (4.22)-(4.24)

$$t = 0, \quad y = 0, \quad y' = y'_0 \quad (4.25)$$

and is controlled by the differential relay so that it performs computation for a certain time  $t_0$  seconds and reset for the following  $t_1$  seconds as shown in the time chart of Fig. 4.12.

Switch S in Fig.4.11 is also controlled by this signal. During the operational period, S is thrown to the left storing  $y - y_0$ , the deviation of the solution from the boundary condition at  $t = t_0$ . During the next reset period the switch is thrown to the right transferring the stored signal on C1 to the feed back capacitor C2 of the accumulator. 68)

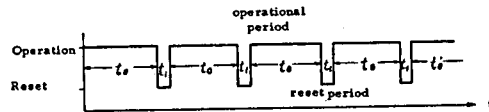


Fig. 4.12 Time chart showing the operational and reset periods of automatic computing circuit.

In the succeeding operational period the output of the accumulator serves as an initial value  $y_0'$ . When boundary condition of eq. (4.24) is not satisfied in an operational period the initial value for the next operational period changes and the different boundary value of  $y$  at  $t = t_0$  will result.

Should the boundary value be satisfied at an operational period no additional signal is added to the accumulator and the output of which remains unchanged.

If this were the case the solutions of the following operational periods are identical and are the required solution. Fig. 4.13 gives an example of the solution and the output of the accumulator.

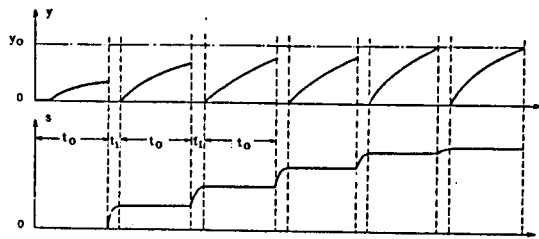


Fig. 4.13 Automatic solution of Eq. (4.22)-(4.24) by the circuit of Fig. 4.11

Usually the output signal of the accumulator is multiplied by a constant factor  $\alpha$  to be used as an input to the analog computer circuit of the differential equation. When  $\alpha$  is large the deviation of the solution from the boundary condition is oscillatory and when  $\alpha$  is small the convergence of the solution is slow and monotonic. It might be probable that the solution is divergent when  $\alpha$  is very large. As will be discovered later the magnitude of  $\alpha$  has a significant effect on the convergence of the automatic programming method.

The principle of this method is not different for the Sturm-Liouville's problem; that is, for differential equation of eq. (4.22) the boundary conditions

$$\text{at } t = 0, \quad y + a_1 y' = b_1 \quad (4.26)$$

$$\text{at } t = t_0, \quad y + a_2 y' = b_2 \quad (4.27)$$

are assigned. This problem is solved automatically by the circuit of

Fig. 4.14, in which the accumulator

accumulates the value of

$(y + a_2 y' - b_2)$  at  $t = t_0$

and feeds its output to  $y_0$  and

$y_0'$  satisfying the relation eq. (4.26).

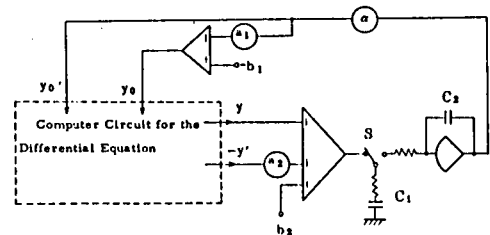


Fig. 4.14 Analog computer circuit for automatic computation of the boundary value problem of eq. (4.26)-(4.27)

As another example the following boundary condition is imposed on the differential equation of eq. (4.22)

$$t = t_1, \quad y = y_1, \quad (4.28)$$

$$t = t_1, \quad y = y'_1. \quad (4.29)$$

The automatic programming circuit is shown in Fig. 4.15.

The stability problem is more serious in these multiple boundary condition problems.

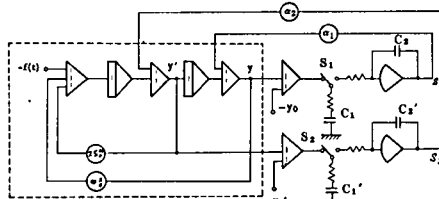


Fig. 4.15 Analog computer circuit for automatic computation of the boundary value problem of eq. (4.22), (4.28) and (4.29)

#### 4.3.2. Eigen Value Problem.

The featuring merit of the automatic programming method is that it is applicable to the eigen value problems. As an example following eigen value problem is solved by the automatic programming method.

$$y'' + \lambda y = 0 \quad (4.30)$$

$$t = 0, \quad y = 0 \quad (4.31)$$

$$t = t_0, \quad y = 0 \quad (4.32)$$

The computing circuit is shown in own

Fig. 4.16. The blocked part of the circuit solves eq. (4.30) with given  $\lambda$  and initial condition of eq. (4.31).

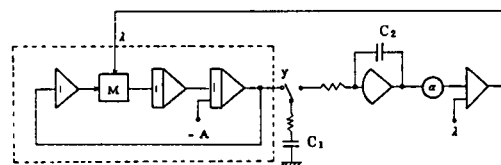


Fig. 4.16 Analog computer circuit for automatic computation of the eigen value problem of eq. (4.30)-(4.32)

At the end of the operational period the deviation of  $y$  from the boundary

condition eq. (4.32) is accumulated in the accumulator which is connected to the multiplier via potentiometer and added to change  $\lambda$ . In this computer circuit the output signal of the accumulator is added to a constant value  $\lambda_0$  to initiate the computation. After a few iteration of the operational periods the solution and the eigen value are automatically obtained. This is shown in Fig. 4.17.

As a final example the equation of motion of a simple

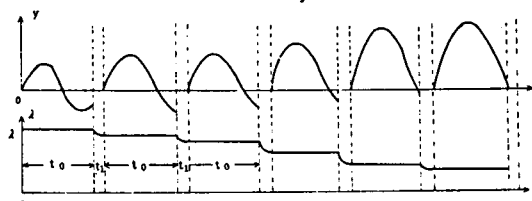


Fig. 4.17 Automatic solution of eq. (4.30)-(4.32) by the circuit of Fig. 4.16

beam simply supported at both ends is solved by the automatic programming.

The differential equation are

$$\frac{d^2 M}{dt^2} + \lambda f(t) Y = 0 \quad (4.33)$$

$$\frac{d^2 Y}{dt^2} + F(t) M = 0 \quad (4.34)$$

and the boundary conditions are

$$t = 0, \quad Y = 0, \quad M = 0 \quad (4.35)$$

$$t = t_0, \quad Y = 0, \quad M = 0 \quad (4.36)$$

As the boundary conditions at the right end are two, two accumulators are needed. The computer circuit is shown in Fig. 4.18. The stability problem

of iteration is more complex in this circuit. By suitable choice of  $\alpha_1, \alpha_2$

and  $\lambda_0$  the iteration converges

and solution is obtained.

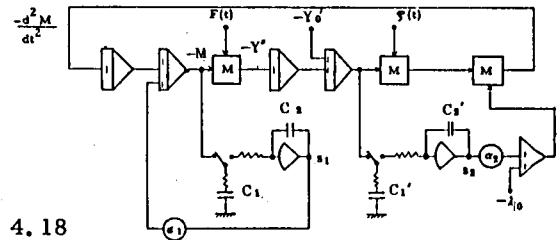


Fig. 4.18

Analog computer circuit for automatic computation of the boundary value problem of eq. (4.33) - (4.36).

#### 4.3.3 Stability Problem of Automatic Programming.

In the preceding examples it was pointed out that the iteration of trials does not always converge, or does not converge to an identical solution. Sometimes the iterations diverge, and sometimes the iterations fall into different solutions depending on the initial condition and the magnitude and sign of  $\alpha$ 's. As the matter of fact the eigen value problem has multiple solutions. The problem of convergence of the automatic programming is now discussed for general two-points boundary value problems.

Consider an ordinary differential equation of order N

$$F(y, y', y'', \dots, y^{(N)}, \lambda, t) = 0 \quad (4.37)$$

With N - p initial conditions at  $t = 0$ ,

$$\varphi_i(y, y', \dots, y^{(N-1)}) = 0 \quad (i=1, 2, \dots, N-p) \quad (4.38)$$

and  $P$  boundary conditions at  $t = t_0$

$$\phi_j(y, y', \dots, y^{(N-1)}) = 0 \quad (j = 1, 2, \dots, P) \quad (4.39)$$

The number of the accumulators required is  $P$ .

The  $(N-P)$  equations for initial conditions of eq. (4.38) are solved for arbitrary  $(N-P)$  initial values  $y(k_1), y(k_2), \dots, y(k_N - P)$ . The remaining  $P$  initial values  $y(k_N - P + 1), \dots, y(k_N)$  are supplied from the accumulators.

The automatic computation circuit of this problem is shown in Fig. 4.19.

Let

$s_{1n}, s_{2n}, \dots, s_{pn}$  denote

the outputs of the accumulators

at the  $n$ th reset period, then

$$s_{jn} = \sum_{k=1}^n \phi_{jk} \quad (j = 1, 2, \dots, P) \quad (4.40)$$

$\phi_{jk}$ , the deviation of boundary condition at the end of  $k$ th operational period is represented as a function of the output of the accumulators at the previous reset period. That is

$$\phi_{jk} = \psi_j(s_{1, k-1}, s_{2, k-1}, \dots, s_{p, k-1}) \quad (4.41)$$

The function  $\psi_j$  is determined by the form of the differential equation,

the initial condition and the boundary condition. From eq. (4.40) and

eq. (4.41)  $s_{jn}$  is written

$$s_{jn} = s_{jn-1} + \psi_j(s_{1n-1}, s_{2n-1}, \dots, s_{pn-1}) \quad (4.42)$$

The stability of the solution of this simultaneous difference equation determines the convergence of the automatic solution of the boundary value problem. Let

$$s_{jn} = s_j^* + \sigma_{jn} \quad (4.43)$$

where

$$\psi_j(s_1^*, s_2^*, \dots, s_p^*) = 0 \quad (4.44)$$

then eq. (4.42) is approximately

$$\sigma_{jn} \cong \sigma_{jn-1} + \frac{\partial \psi_j^*}{\partial s_1} \sigma_{1n-1} + \frac{\partial \psi_j^*}{\partial s_2} \sigma_{2n-1} + \dots + \frac{\partial \psi_j^*}{\partial s_p} \sigma_{pn-1} \quad (j = 1, 2, \dots, P) \quad (4.45)$$

$$\text{where} \quad \frac{\partial \psi_j^*}{\partial s_i} = \left( \frac{\partial \psi_j}{\partial s_i} \right)_{s_1 = s_1^*, \dots, s_p = s_p^*} \quad (4.46)$$

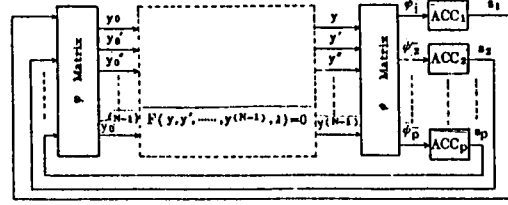


Fig. 4.19 Circuit for automatic computation of the boundary value problem of eq. (4.37)-(4.39)

eq. (4.45) is a linear simultaneous difference equation which is, in vectorial form

$$\begin{pmatrix} \sigma_{1n} \\ \sigma_{2n} \\ \vdots \\ \sigma_{pn} \end{pmatrix} = \begin{pmatrix} \sigma_{1n-1} \\ \sigma_{2n-1} \\ \vdots \\ \sigma_{pn-1} \end{pmatrix} + \begin{pmatrix} \frac{\partial \psi_1}{\partial s_1} & \frac{\partial \psi_1}{\partial s_2} & \dots & \frac{\partial \psi_1}{\partial s_p} \\ \frac{\partial \psi_2}{\partial s_1} & \frac{\partial \psi_2}{\partial s_2} & \dots & \frac{\partial \psi_2}{\partial s_p} \\ \vdots & \vdots & \ddots & \vdots \\ \frac{\partial \psi_p}{\partial s_1} & \frac{\partial \psi_p}{\partial s_2} & \dots & \frac{\partial \psi_p}{\partial s_p} \end{pmatrix} \begin{pmatrix} \sigma_{1n-1} \\ \sigma_{2n-1} \\ \vdots \\ \sigma_{pn-1} \end{pmatrix} \quad (4.47)$$

Substituting

$$\sigma_{jn} = \mu \sigma_{jn-1} \quad (j = 1, 2, \dots, p) \quad (4.48)$$

into eq. (4.47) the following secular equation is obtained.

$$\left| (1 - \mu) E + \left( \frac{\partial \psi_i}{\partial s_j} \right) \right| = 0 \quad (4.49)$$

Only when  $|\mu| < 1$   $\sigma_{jn}$  converges to zero and the automatic computation is stable.

EX. 4. 1 The convergence of the boundary value problem

$$y'' + 2 \zeta \omega_0 y' + \omega_0^2 y = f(t) \quad (4.50)$$

$$t = 0, \quad y = 0$$

$$t = t_0, \quad y = y_1$$

which was solved by the automatic computing circuit of Fig. 4.11 is examined. In this case

$$N = 2, \quad p = 1 \quad (4.51)$$

and initial condition is

$$\varphi(y, y') = y = 0 \quad (4.52)$$

and the boundary condition at the right end is

$$\psi(y, y') = y - y_1 = 0 \quad (4.53)$$

$\phi_n$ , the value of  $\psi(y, y')$  at the end of  $n$ th operational period is

$$\phi_n = y_n - y_1 \quad (4.54)$$

and  $y_n$  is a linear function of  $y_0'$ , the initial value of  $y'$  at  $t = 0$ , as

$$y_n = A y_0' + B$$

$y'_0$  is supplied by the output of the accumulator like

$$y' = \alpha s_n \quad (4.55)$$

According to eq. (4.40)

$$s_n = \sum_{k=1}^n \phi_k \quad (4.56)$$

$$\phi_k = y_n - y_1 = A \alpha s_n + B - y_1 \quad (4.57)$$

Therefore the following difference equation corresponding eq. (4.42) results.

$$s_n = (1 + \alpha A) s_{n-1} + B - y_1 \quad (4.58)$$

The characteristic root of this difference equation is

$$\mu = (1 + \alpha A) \quad (4.59)$$

When  $|\mu| < 1$  the automatic computation converges. This condition

corresponds to the following condition for  $\alpha$

$$\left. \begin{array}{l} \text{if } A > 0 \quad -\frac{2}{A} < \alpha < 0 \\ \text{if } A < 0 \quad 0 < \alpha < \frac{2}{A} \end{array} \right\} \quad (4.60)$$

The stability of the iteration is best explained by the graphical method.

In Fig. 4.20  $s_n$  is plotted against  $s_{n-1}$  by eq. (4.58).

Straight line A representing eq. (4.58)

gives the output of the accumulator

at the  $n$ th reset period when that

of the previous reset period is  $s_{n-1}$

By using another straight line B

representing  $s_n = s_{n-1}$ , is

obtained from  $s_n$ .

When in the  $n$ th reset period

$s_{n+1}$  is represented by the

ordinate of point Q1, or by

point P2 on the straight line

B.  $s_{n+1}$  is then represented

by the ordinate of point Q2 of

which abscissa is the ordinate

of P2.

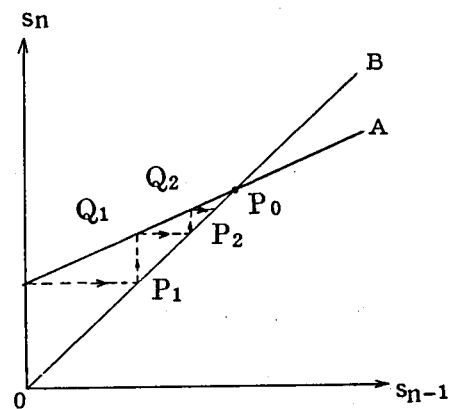


Fig. 4.20

Relationship between  $s_n$  and  $s_{n-1}$ , the output signals of the accumulator for successive two iteration periods. A represents relation of eq. (4.58), whereas B represents the relation

$$s_n = s_{n-1}$$



Thus  $s_n$  converges to the point  $P_0$  where A and B cross. Depending on the magnitude and sign of  $\alpha$  the relative position of A and B changes as shown in Fig. 4.21.

In (a),  $0 < 1 + \alpha A < 1$   
and the iteration converges  
monotonically, in (b),

$$-1 < 1 + \alpha A < 0$$

and the iteration converges  
oscillatory, in (c),

$$1 + \alpha A > 1 \quad \text{and}$$

the iteration diverges

monotonically, and in (d)

$$1 + \alpha A < -1 \quad \text{and}$$

the iteration diverges

oscillatory.

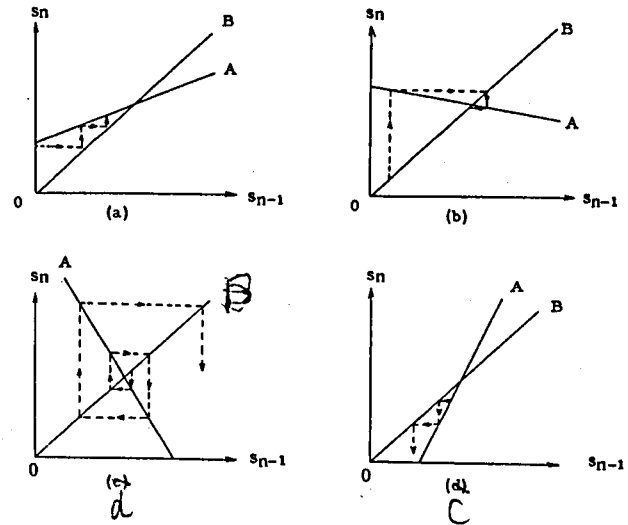


Fig. 4.21 Relative position of A and B.

(a) $0 < 1 + \alpha A < 1$	: stable
(b) $-1 < 1 + \alpha A < 0$	: stable
(c) $1 < 1 + \alpha A$	: unstable
(d) $1 + \alpha A < -1$	: unstable

EX. 4. 2 Let us then examine the stability problem of two point boundary value problem of the second order differential equation

$$y'' + 2\mathcal{S}\omega_0 y' + \omega_0^2 y = f(t) \quad (4.61)$$

$$t = t_0 \quad y = y_1 \quad (4.62)$$

$$t = t_0 \quad y' = y'_1 \quad (4.63)$$

for which

$$\phi_1 = y(t_0) - y_1 \quad (4.64)$$

$$\phi_2 = y'(t_0) - y'_1 \quad (4.65)$$

For the convenience of discussion it is decided to supply initial value of  $y$  from the first accumulator and that of  $y'$  from the second accumulator. The values of  $y$  and  $y'$  at  $t = t_0$  are written

$$y(t_0) = A y_0 + B y'_0 + C \quad (4.66)$$

$$y'(t_0) = A' y_0 + B' y'_0 + C' \quad (4.67)$$

In the  $n$  th operational period

$$y_o = \alpha_1 s_{1n} \quad (4.68)$$

$$y_o' = \alpha_2 s_{2n} \quad (4.69)$$

From these relations difference equation for  $s_{1n}$  and  $s_{2n}$  is derived as follows

$$\begin{aligned} s_{1n} &= s_{1n-1} + \phi_{1n} \\ &= s_{1n-1} + A\alpha_1 s_{1n-1} + B\alpha_2 s_{2n-1} + C - y_1 \\ &= (1 + A\alpha_1)s_{1n-1} + B\alpha_2 s_{2n-1} + C - y_1 \end{aligned} \quad (4.70)$$

$$\begin{aligned} s_{2n} &= s_{2n-1} + \phi_{2n} \\ &= s_{2n-1} + A'\alpha_1 s_{1n-1} + B'\alpha_2 s_{2n-1} + C' - y_1' \\ &= A'\alpha_1 s_{1n-1} + (1 + B'\alpha_2)s_{2n-1} + C' - y_1' \end{aligned} \quad (4.71)$$

The characteristic equation of the above simultaneous difference equation is

$$\begin{vmatrix} (1 + A\alpha_1) - \mu & B\alpha_2 \\ A'\alpha_1 & (1 + B'\alpha_2) - \mu \end{vmatrix} = 0 \quad (4.72)$$

Suitable values of  $\alpha_1$ , and  $\alpha_2$  which make the iteration convergent are selected to satisfy eq. (4.72) for  $|\mu| < 1$ .

EX. 4.3. As a final example the stability of eigen value problem solved by the circuit of Fig. 4.16 is examined. In this example

$$\phi_n = y_n = \frac{A}{\sqrt{\lambda_n}} \sin \sqrt{\lambda_n} \cdot t. \quad (4.73)$$

where

$$\lambda_n = \lambda_o + \alpha s_{n-1} \quad (4.74)$$

then

$$s_n = s_{n-1} + \frac{A}{\sqrt{\lambda_o + \alpha s_{n-1}}} \sin \sqrt{\lambda_o + \alpha s_{n-1}} \cdot t. \quad (4.75)$$

or denoting

$$\sigma_n = \lambda_o + \alpha s_n \quad (4.76)$$

eq. (4.75) is rewritten as

$$\sigma_n = \sigma_{n-1} + \frac{\alpha A}{\sqrt{\sigma_{n-1}}} \sin \sqrt{\sigma_{n-1}} \cdot t. \quad (4.77)$$

Eq. (4.77) is plotted in Fig. 4.22. This curve crosses straight line of

$$\sigma_n = \sigma_{n-1} \text{ at multiple points A, B, C, } \dots$$

The stability is locally investigated for these points. Point A corresponds to Fig. 4.21 (b) and point B to Fig. 4.21 (c) and both points are unstable and point C to (a) which is stable.

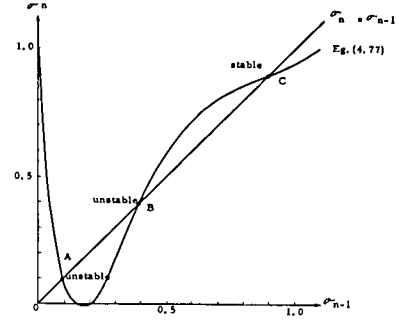


Fig. 4.22 Relationship between  $\sigma_n$  and  $\sigma_{n-1}$  of eq. (4.77) for  $A = 1/t_1$ .

The stationary values of  $\sigma$  are calculated from Eq. (4.77) by putting  $\sigma_n = \sigma_{n-1} = \sigma$ , as

$$\sigma_N = \left(\frac{N\pi}{t_1}\right)^2 \quad (N = 1, 2, \dots) \quad (4.78)$$

Put  $\sigma_n - \sigma_N = \varepsilon_n$  eq. (4.77) is then written

$$\begin{aligned} \varepsilon_n &= \varepsilon_{n-1} + \frac{\alpha A}{\sqrt{\sigma_N + \varepsilon_{n-1}}} \sin \sqrt{\sigma_N + \varepsilon_{n-1}} \cdot t_1 \\ &\approx \left\{ 1 + \frac{(-1)^N t_1^3}{2(N\pi)^2} \alpha A \right\} \varepsilon_{n-1} \end{aligned} \quad (4.80)$$

The stability condition is then obtained as follows

$$\left. \begin{array}{ll} \text{For } A & \text{and even } N \quad -\frac{2\sigma_N}{At_1} < \alpha < 0 \\ \text{"} & \text{and even } N \quad 0 < \alpha < \frac{2\sigma_N}{At_1} \\ \text{For } A & \text{and even } N \quad 0 < \alpha < -\frac{2\sigma_N}{At_1} \\ \text{"} & \text{and even } N \quad \frac{2\sigma_N}{At_1} < \alpha < 0 \end{array} \right\} \quad (4.81)$$

#### 4.4 Calculation of the Transfer Function of Noisy Processes by the Delay Line Filter. 69)

The delay line filter has been found useful for detecting the periodic signal from a noisy channel when its frequency is exactly known. 70)83)84)

The block diagram of the delay line filter is shown in Fig. 4.23. The delay time of the delay line is exactly the same to the period of the periodic signal to be detected.

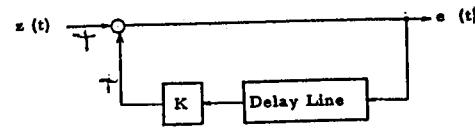


Fig. 4.23 Delay line filter.

The gain of the delay line filter for the periodic signal is calculated as

$$H = \frac{1}{1 - K} \quad (4.82)$$

and the gain for the signal to noise ratio is calculated as

$$G = 10 \log_{10} \left( \frac{1 + K}{1 - K} \right) \text{ dB} \quad (4.83)$$

Table 4.1

Signal amplification and S/N improvement of the delay line filter.

K	gain of signal amplification	rate of S/N improvement	gain of S/N improvement
0.90	10	4.35	12.8 dB
0.95	20	6.25	15.9
0.98	50	9.95	20
0.99	100	14.1	23
0.9999	10,000	141.4	43

The gain in signal to noise ratio for various gain K is shown in Table 4.1 with the amplification factor for the periodic signal.

The delay line filter can be used to the measurement of the transfer function of a process or control elements. The delay lines of sampling principle use gate signal to sample the input signal and store in the storage elements. This gate signal is used to generate a periodic signal of which period is identical to the delay time of the delay line. By suitable filter this periodic signal is transformed into a proper waveform and then introduced into the process under measurement. When this is a pulse train

the response of the process is the weighting function, and when this is a sinusoidal wave the response is the frequency response. Generally the transfer function of the process is obtained from the Fourier transform of the input signal  $f(t)$  and that of the output signal  $e_o(t)$ .

$$G(2\pi jf) = \frac{E_o(2\pi jf)}{F(2\pi jf)} \quad (4.84)$$

where  $F(2\pi jf)$  and  $E_o(2\pi jf)$  denote Fourier transform of  $f(t)$  and  $e_o(t)$  respectively.

As ~~usually~~ <sup>usually</sup> the output signal from the process is noisy, this is fed into the delay line filter and the obtained noiseless signal is used for the analysis. A program for obtaining the transfer function of the process from the waveform of  $f(t)$  and  $e_o(t)$  is prepared. In this program the Fourier transform of the sampled function  $e_o(t)$  is calculated by the following semi-analytic formula

$$\begin{aligned} E_o(j\omega) &= \int_0^{\infty} e_o(t) e^{-j\omega t} dt \\ &\equiv \sum_{n=0}^N e_o(n\Delta) \int_{(n-\frac{1}{2})\Delta}^{(n+\frac{1}{2})\Delta} e^{-j\omega t} dt \\ &= \frac{2}{\omega} \sin \frac{\omega\Delta}{2} \cdot \sum_{n=0}^N e_o(n\Delta) e^{-j\omega n\Delta} \end{aligned} \quad (4.85)$$

The input signal to the process is either square pulse like one in Fig. 4.24 or arbitrary time function. The prepared program is capable of handling either type of the input signals. The data card for this program should be punched in the format of (5F 10.4).

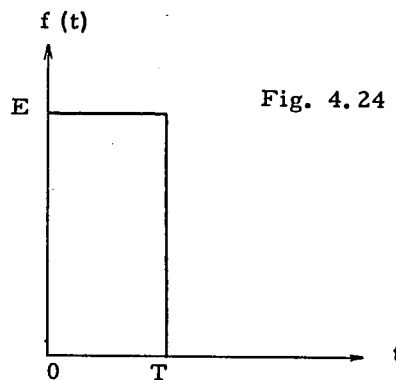


Fig. 4.24 Square Pulse.

"The first card should carry index of input signal waveform, which is 1 when it is square pulse and is 0 when it is arbitrary time function, sampling interval  $\Delta$  (sec.), pulse height  $E$  and the pulse width  $T$  (sec.). The following four cards should carry twenty frequencies in cps for which the transfer function is wanted. The next ten cards should carry sampled input waveform  $f(0), f(4), f(24), \dots, f(49\Delta)$ . The last ten cards should carry sampled output waveform  $e_0(0), e_0(\Delta), e_0(2\Delta), \dots, e_0(49\Delta)$ ".

The result of computation is printed in a way as the first line is the the data of the first input card in the format of ( 5 F 20.4), the next twenty lines show the frequency, gain of the transfer function in dB, phase in degree,

$|F(2\pi if)|$  dB, and  $|E_0(2\pi if)|$  dB in the format of ( 3 F 15.2, F 20.2, F 10.2).

Examples of the output signal of the delay line filter are shown in

Fig. 4.25

RESPONSE OF THE DELAY LINE FILTER SUBJECT TO THE SINUSOIDAL INPUT

Delay time = 1.89 seconds

$K = 0.95$

(a)  $f = 0.57 = \frac{1}{1.75}$  c/s

(b)  $f = 0.53 = \frac{1}{1.89}$  c/s

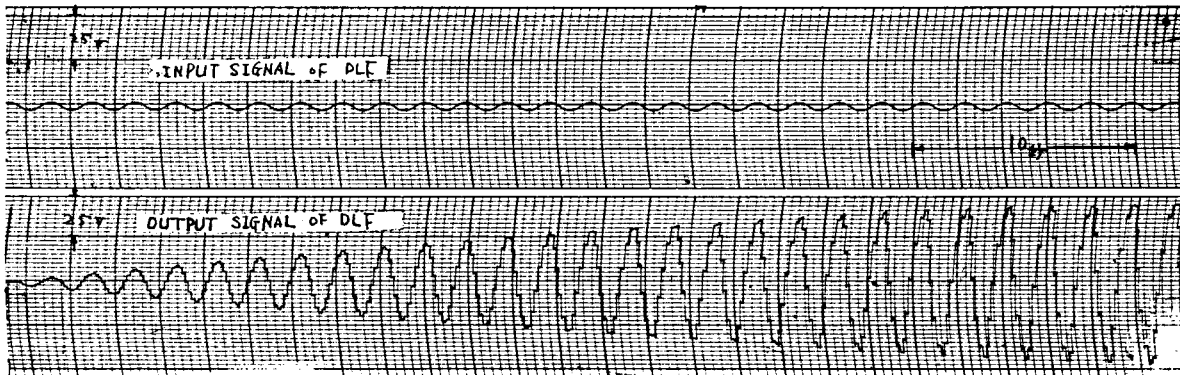
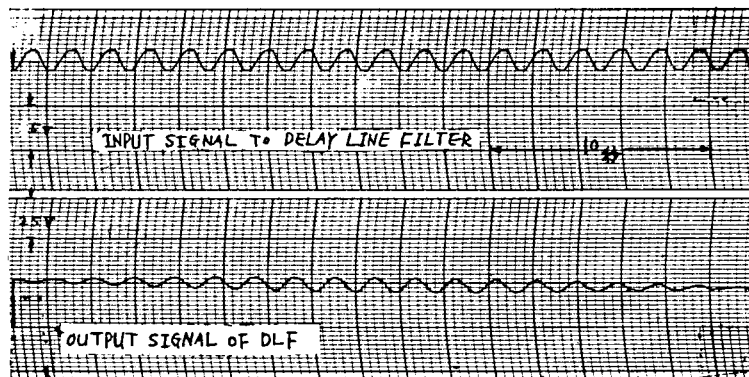


Fig. 4.25 outputs of the delay line filter subject to the sinusoidal input signal of different frequencies are shown. In case the period of the input signal is identical to the delay time of the delay line this signal is amplified, while for the signals of different period the amplification does not take place. From the waveform of Fig. 4.26 a large time constant of the delay line filter is observable. As the transfer function of the delay line filter is given by

$$\frac{E_o(s)}{Z_i(s)} = \frac{1}{1 - Ke^{-\tau s}} \cong \frac{1}{1 - K} \cdot \frac{1}{1 - \frac{K\tau}{1-K}s} \quad (4.86)$$

the time constant is obtained as

$$T = \frac{K\tau}{1 - K} \quad (4.87)$$

As K approaches unity the time constant grows to infinity.

In Fig. 4.26 an example of measuring step reponse of a unit lag element is shown. A train of square pulses with the duration of fifty per cent and the period identical to the delay time of the delay line is applied to an analog computer representing a unit lag. The output from the analog computer circuit is mixed with a random noise from a noise generator and is fed into the delay line filter. As is clearly observed in Fig. 4.26. the noise is almost removed from the output of the delay line filter. Also shown in Fig. 4.27. is the output of the delay line filter with greater amount of noise in input signal. In the original signal the periodic signal is hardly recognizable, while the output signal of the delay line filter is considerably purely periodical.

The limit of this measurement of the transfer function by the delay line filter should be mentioned. To maintain the accuracy of the result of calculation of the transfer function by eq. (4.97) the pulse width T should satisfy the following inequality

$$T < \frac{1}{f_o} \quad (4.88)$$

where  $f_0$  is the highest frequency for which the transfer function is wanted, because  $|F(2\pi if)|$  is zero at  $1/T$  cps and causes large error in calculation of  $G(2\pi if)$ .

Although the above example is on the determination of known transfer function on analog computer the use of the delay line filter is considerably effective to the identification of the transfer function of the actual physical system. Of particular interest<sup>04</sup> is the frequency response measurement using the delay line filter. Input signal to the noisy process is sinusoidal signal of which period is identical to the delay time of the delay line. As the delay time of the delay line is changed the period of the sinusoidal signal also changes and the response of the process to the sinusoidal input signal for different frequencies is obtained. For instance the accuracy of the pile oscillator will be greatly improved. Another promising application of the delay line filter in the measurement of locally linearized transfer function of nonlinear processes as very small input signal is sufficient for this method.



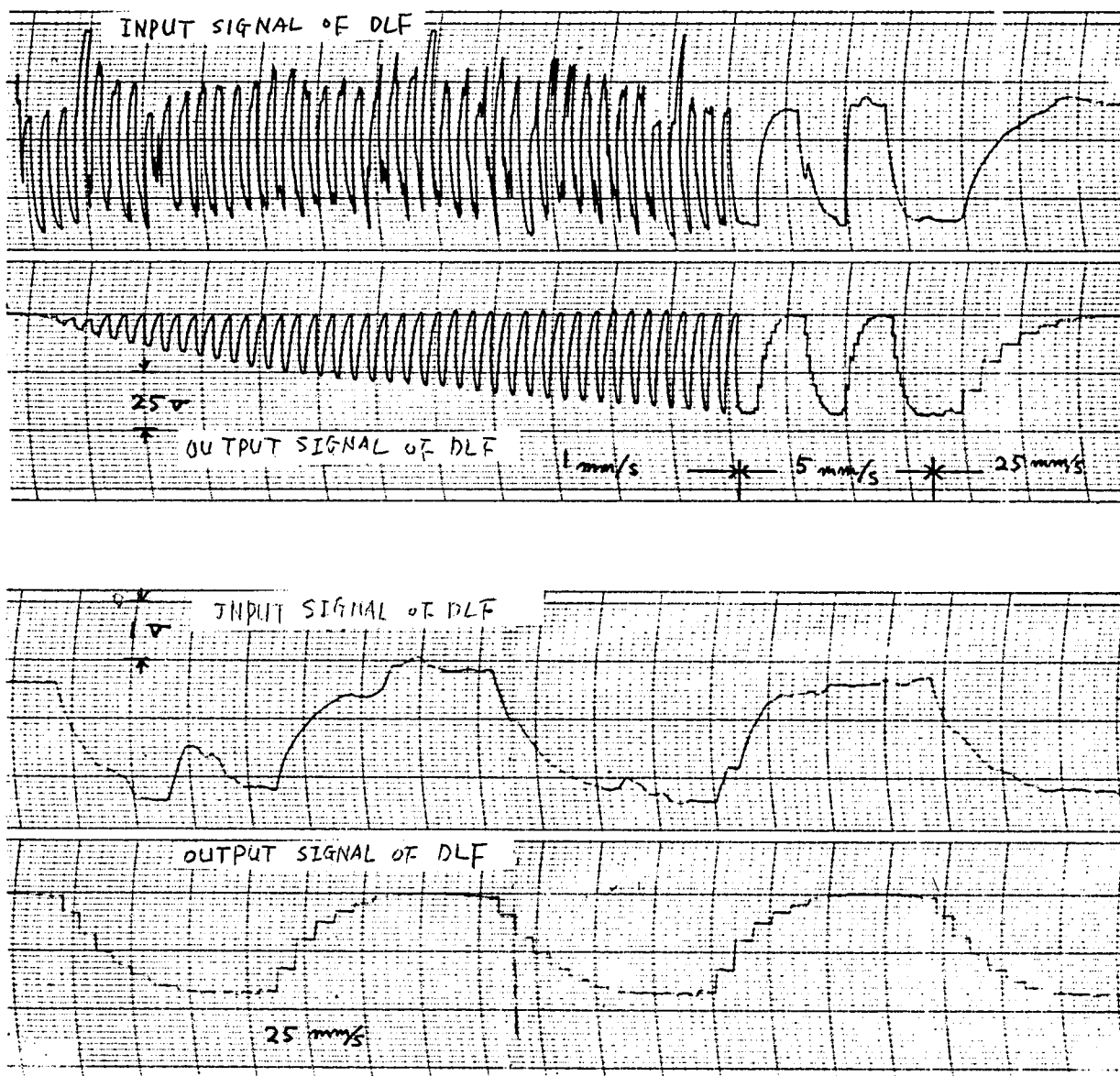


Fig. 4.26

EXAMPLE OF MEASURING STEP RESPONSE OF A PROCESS WITH NOISE

Transfer function of the process :  $\frac{1}{1 + 0.5s}$

Delay time of delay line : 3 seconds

K : 0.96

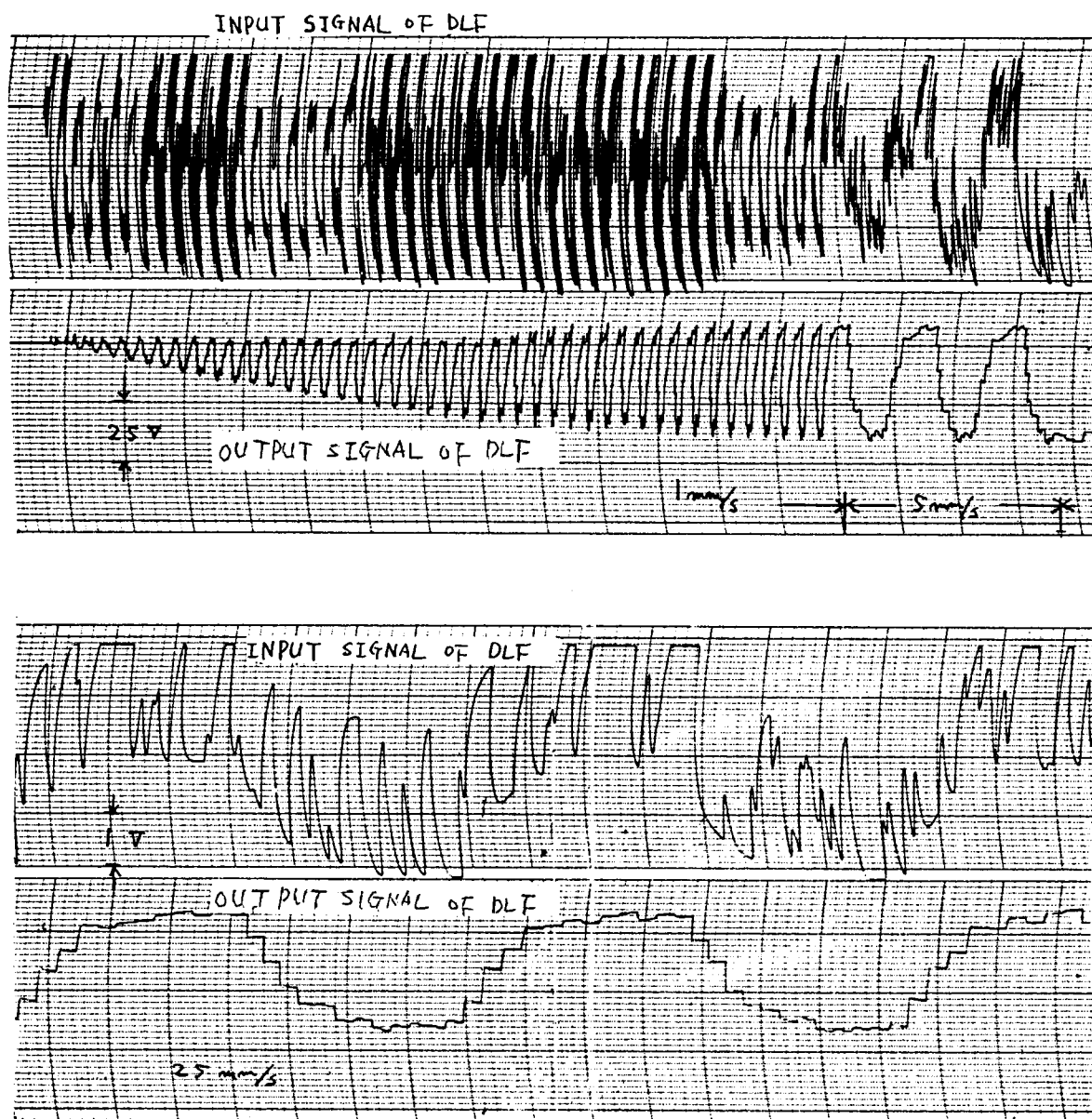


Fig. 4.27

EXAMPLE OF MEASURING STEP RESPONSE OF A PROCESS  
WITH LARGE NOISE

Transfer function of the process :  $\frac{1}{1 + 0.5s}$

Delay time of delay line : 3 seconds

K : 0.96

## 5.1 Introduction

In the earlier age of the electronic computers discussions were mainly on the advantage and disadvantage of the analog computer and the digital computer. Those discussions were never concluded as long as we stick to a conventional type of operation of either type of the computers.

The advantages of the analog computer are as follow.

- (1) The programming is relatively easy. For solving a differential equation of the order more than twenty the programmer only draws a block diagram and sets up the wiring on the patch board.
- (2) The accuracy of the obtained result by the analog computer is from one to two percent which is sufficient for usual purposes.
- (3) One can simulate a dynamic system on the analog computer without deriving the differential equation of the system.
- (4) Analog computer circuit is useful for investigating the effect of the effect of the change of the parameters to the response of the system.
- (5) The speed of computation of the analog computer is much larger than that of the digital computer.
- (6) The solution of the analog computer is obtained in the form of graphs.
- (7) Cost is less.

The analog computer has many disadvantages, too, as the merits sometimes <sup>it</sup> turn out to be demerits depending on the application. They are as follow.

- (1) The analog computer is almost powerless to the mathematical problems other than the ordinary differential equation. Although it is sometimes useful to algebraic equations and partial differential equations the method of application is neither extensive nor flexible.

- (2) More than 0.1 % of accuracy is hardly obtainable by the analog computer. As is shown in Fig. 5.1 digital computer is favorable for more elaborate calculation.

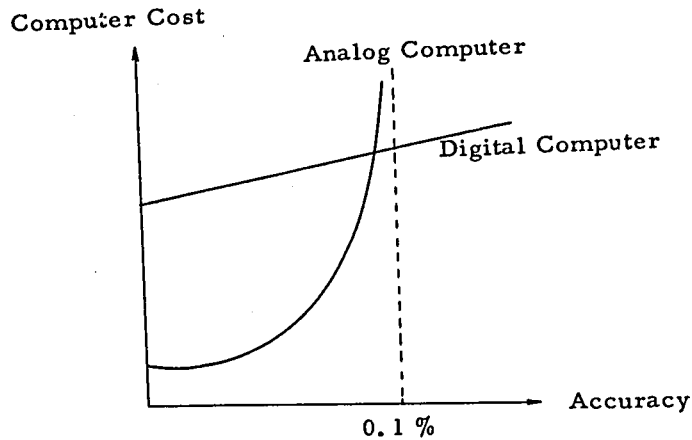


Fig. 5.1 Computer cost vs accuracy

- (3) The origin of the error in analog computer is complex and the prediction and the correction of the error are often unfeasible.
- (4) The manual setting of the parameters and zero-balancing of operational amplifiers often induce misoperation.
- (5) Operation of decision is difficult. Changing the program of the calculation in the course of computation subject to intermediate results by the computer itself is difficult. The automatic programming method described in 4.3 is an attempt to overcome this difficulty, but this is not a general solution of the problem.
- (6) Multiplier, divider and function generator of the analog computer are not satisfactory relative to high precision linear elements.
- (7) The fact that time is the only independent variable in analog computer restricts the programming technique.

To compare with the analog computer the advantages and disadvantages of the digital computer are briefly reviewed.

The advantages of the digital computer are as follow.

- (1) Digital computers are used in almost any mathematical problems.

- (2) Any accuracy as desired is obtainable. The error of the calculated result is determined and is estimated mathematically.
- (3) Decision is capable in the digital computer and enables flexible programming.
- (4) Parameter of the equation is automatically calculated from the input data.
- (5) Input and output equipments are more capable than those of the analog computer keeping off the problem analyst from time consuming data processing and parameter setting.

- (6) The solution is obtained in the form of the table.

The disadvantages of the digital computer are as follow.

- (1) Debugging of the program takes considerable time.
- (2) Programming is less easy than analog computer.
- (3) When solving the differential equation the computation speed is much slower than the analog computer.
- (4) When investigating the dynamic property of a physical system the simulation technique of analog computer is inapplicable.

Regarding the recent development of the analog computer one of the major currents such as the large scale machines and the transistorization is automatic computation technique. By this technique parameters of the equations as initial values and coefficients are changed automatically until the solution satisfying certain boundary condition is obtained, or computed result is transformed into digital form by analog-to-digital converter and printed by typewriter. These attempts are to approach analog computer to digital computer. However, as the analog computer uses the physical property of the circuit element for the computation a certain amount of error is intrinsic and the analog computer can never be a digital computer.

A general purpose digital computer has many superiority to the

analog computer, but from the point of view of a differential analyzer, is inferior. An attempt has been tried to provide a digital computer with the ability of the differential analyzer. It is the digital differential analyzer which is manufactured by Bendix and Litton Companies. 76)77)78)

The principle of the digital differential analyzer is more alike that of the general purpose digital computer. In the digital differential analyzer registers corresponding to integrators are stored in magnetic drum and the stored information is read out at every revolution of the drum and the step of integration proced<sup>ed</sup>~~es~~. The result of the integration of each step is again stored in the drum. The time required to execute a step of integration (iteration time) is the time of one revolution of the magnetic drum. When the speed of the drum is 1,500 rpm the iteration time is 40 ms which means more than an hour is required for 100,000 steps of integration.

The program of the digital differential analyzer is punched on tape and is fed into the magnetic drum. This makes the change of the program difficult. In many cases the initial values are erased after each run, so that it requires to feed initial values at every run of the computation. The digital differential analyzer is therefore more alike the general purpose digital computer and has less merit of the analog computer. The computation times of a certain problem by different type of computers were reported as shown in Table 5.1. 79)

Table 5.1  
Computation times and costs of different types of computers

Type of Computers	Time spent for Programming	Computer Time	Cost
REAC Analog Computer	2 hr.	50 mm	\$ 53
Litton DDA	8 hr.	20 hr.	\$ 280
IBM 704	2 wrs	50 min.	\$1377
Hand Calculation.	1 day	3 wks	\$1295







Being unsatisfied with the digital differential analyzer the author has designed a new digital computer provided with the high computation speed of the analog computer and the high precision of the digital computer. The author named this new computer the Digitalized Analog Computer, or in abbreviation, DAC. In the final feature of DAC, it will receive analog input and produce analog output so that it will be connected with the analog computer. At the present moment, however, the input signal is given by octal switch and only analog output is obtainable.

## 5.2 System Design

### 5.2.1 General Description of DAC

DAC is constructed from a set of computing elements shown in Table 5.2 which are connected on the connecting board according to the problem as is done in analog computers.

Table 5.2  
DAC Computer elements

No.	Element	Symbol	Operation
1	Integrator		$dZ = \pm Z^k \cdot Y \cdot dx$ $Y = \int dy$
2	Coefficient Multiplier		$dY = k dx$ $ k  < 1$
3	Servo Element		$dz = \begin{cases} 2^{-10} \cdot \sum dy_i > 0 \\ 0 & = 0 \\ -2^{-10} & < 0 \end{cases}$
4	Adder		$dZ = \frac{1}{2} (dy_1 + dy_2)$
5	Multiplier		$dZ = U dV + V dU + dU dV$
6	Switch Element		$U > V \quad 1 = 2$ $U < V \quad 1 = 3$

The initial values of integrater, adder and multiplier and the multiplication factor of coefficient multiplier are given by octal switches of each element. These elements perform the operation eventually in synchronization with the clock pulse of 100 kcps distributed from the control circuit. Output signal from the element is pulses produced every iteration time and eventually serves as an input signal to other elements. The result of computation is either converted into analog voltage by D-A converter and recorded by pen oscillograph or printed in digital form.

Inside the computing element mathematical operations such as inte-

gration, addition, coefficient multiplication, variable multiplication and decision are approximated by difference equation and are executed digitally step by step. Generally the computing element has two registers which store variable of the present step and that of the preceding step respectively and repeats the operation of adding the content of one register to that of the second register in every iteration time.

From the nature of the difference equation approximation of the differential equation smaller the magnitude of the step more accurate is the result. However, as the magnitude of the step decreases, the number of step necessary to perform the integration for a certain interval increases resulting a decrease in the computation speed. The relationship between the accuracy and the computation speed is discussed in the later section.

### 5.2.2 Number System

The number system in the computing elements is as follows

one word	=	serial pure binary number
		18 bits + sign bit + space = 20 bits
negative number	=	two's complement
clock frequency	=	100 kc
iteration time	=	0.2 ms ( = 5000 steps per second)

The number is a serial binary number as shown in Fig. 5.2.

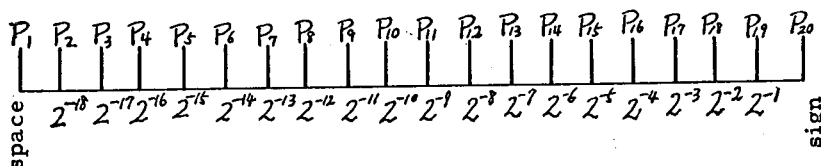


Fig. 5.2 Timing Pulse

The space bit precedes number bits which appear with the least signifi-



cant bit first and the most significant bit last. The last bit of a word is the sign bit. The number is represented by fixed point. The number never surpass unity in absolute value. The first number bit always designates  $2^{-18}$  and the last number bit  $2^{-1}$ . Each bit of the word is called the timing pulse and is named P1, P2, ..., P20. When the sign bit is one the number is negative and when it is zero the number is positive.

### 5.2.3 Integrater

The principle of operation of DAC is best explained by the integrater. Other computing elements such as multiplier, coefficient multiplier and adder are the modifications of the integrater.

Among the many ways of approximating the differential equation

$$\frac{dZ}{dX} = Y \quad (5.1)$$

by the difference equation Euler's formula and trapezoidal formula are feasible ones. Although DAC uses the trapezoidal formula, the principle of operation of DAC is provisionally explained by Euler's formula first.

#### (i) Integrater by Euler's formula

The difference equation approximation of the differential equation of eq. (5.1) by Euler's method is as follows.

$$Z_{n+1} = Z_n + Y_n \Delta X_n \quad (5.2)$$

Consider two registers which store  $Z_n$  and  $Y_n$  respectively and the stored numbers are in fixed point binary number. Let

$$\Delta X_n = 2^{-k} \quad (5.3)$$

then the operation of eq. (5.2) simply means that the content of  $Y_n$  register is shifted  $k$  places to the right and added to the content of  $Z_n$  register. The magnitude of  $k$  determines the accuracy of the computation. For the convenience of the circuitry  $k$  is selected to be  $N$  which is the half of the number of bits of the registers. Therefore

$$\Delta X_n = 2^{-N} \quad (5.4)$$

Then the operation of eq. (5.2) means that left half of the content of  $Y_n$  register is added to the right half of the  $Z_n$  register. Hence  $Z_n$  and  $Y_n$  registers are conceptually separable into upper and lower parts the length of which is  $N$ . To the upper register the carry from the lower register is sent and the content of the upper register is added to another lower register. Denoting the upper register  $Y$  register and the lower register  $R$  register an integrater is composed of them in a way shown in Fig. 5.3.

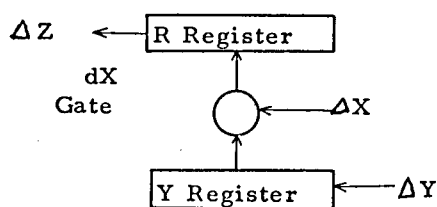


Fig. 5.3 Euler integrater

As  $X$  increases  $\Delta X (= 2^{-N})$  content of  $Y$  register is added into  $R$  register and when the content of  $R$  register surpasses unity positive carry is emitted and when it becomes less than zero negative carry is emitted. This signal from the  $R$  register is  $\Delta Z$  signal and serves as an input to the  $Y$  register of other integrater. As a result  $R$  register stores remainder of  $Z$  and the  $Y$  register stores significant bits of  $Z$ .  $dX$  gate of the integrater as shown in Fig. 5.3 works such that

- |                                |                           |
|--------------------------------|---------------------------|
| (1) $Y$ is added to $R$        | when $\Delta X = 2^{-N}$  |
| (2) $Y$ is subtracted from $R$ | when $\Delta X = -2^{-N}$ |
| (3) No operation is performed  | when $\Delta X = 0$       |

The function of the integrater is shown in Table 5.3 below.

Table 5.3

$R_n + Y_n \Delta X_n$	$R_{n+1}$	$\Delta Z_{n+1}$
$0 \leq \text{ , and } < 1$	$R_n + Y_n \Delta X_n$	0
$\geq 1$	$R_n + Y_n \Delta X_n - 1$	$2^{-N}$
$< 0$	$R_n + Y_n \Delta X_n + 1$	$-2^{-N}$

(ii) Integrater by Trapezoidal Formula

Instead of using Euler's formula for approximating the integration DAC uses the trapezoidal integration formula for attaining higher accuracy.

The trapezoidal formula is

$$Z_{n+1} = Z_n + Y_n \Delta X_n + 1/2 (Y_n - Y_{n-1}) \Delta X_n \quad (5.5)$$

or by incremental expression

$$\Delta Z_{n+1} = Y_n \Delta X_n + \frac{1}{2} \Delta Y_n \Delta X_n \quad (5.6)$$

where

$$\Delta Z_n = Z_n - Z_{n-1} \quad (5.7)$$

$$\Delta Y_n = Y_n - Y_{n-1} \quad (5.8)$$

The block diagram of the trapezoidal integrater is shown in Fig. 5.4.

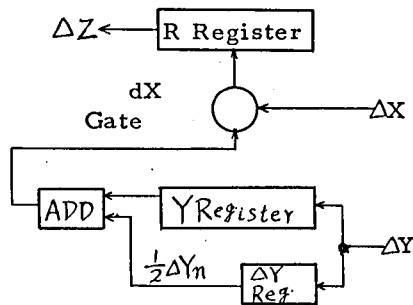


Fig. 5.4 Trapezoidal integrater

The Y register in the block diagram is a two-bit accumulator producing a positive output signal and resetting the contents when the contents become two and producing a negative output signal and resetting the contents when the contents become minus two. The operation of the Y register is described by Table 5.4.

Table 5.4

$\{\Delta Y\}_{n-1} + \Delta Y_n$	$\{\Delta Y\}_n$	$1/2 \Delta Y_n$
$0, 2^{-N} \text{ or } -2^{-N}$	$\{\Delta Y\}_{n-1} + \Delta Y_n$	0
$2^{-N+1}$	0	$2^{-N}$
$-2^{-N+1}$	0	$-2^{-N}$

According to the block diagram of the trapezoidal integrater of Fig. 5.4, when  $\Delta Y$  is sent into an integrater while  $\Delta X$  is not given, the output of  $\Delta Y$  register is not used and the trapezoidal correction is not performed. To avoid this contradiction the trapezoidal integrater shown in the block diagram of Fig. 5.5 may be used. In the latter integrater an auxilliary register stores  $1/2 \sum \Delta Y$ , and is reset by  $\Delta X$ . In usual computer circuit, however, the absence of  $\Delta X$  instead of  $\Delta Y$  is seldom and the former type of the trapezoidal integrater is employed in DAC.

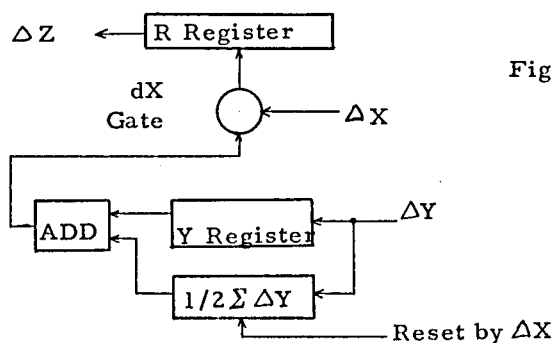


Fig. 5.5 Alternative form of the trapezoidal integrater.

### (iii) Length of Variables

The length of the register of DAC is fixed at eighteen bits. In the actual operation the effective length of the register, or the length of the variable is changed depending on the required speed and the accuracy of the computation. When the content of Y register is small  $\Delta Z$  is not generated for a long time until it is added to R register a considerable number of times which causes slow computation speed. When  $\Delta Y$  is added to the upper bits of the Y register the computation speed increases, but the length of the Y register decreases causing poorer accuracy. This complementary relation of the accuracy and the speed of computation is unavoidable and is essential in the incremental computers including DAC. The only way to get around this is to increase the clock frequency.

When  $\Delta Y$  is added to the  $(k + 1)$  th bit from the bottom of the Y register the operational equation of the integrater is

$$Z = 2^k ( Y + 1/2 \Delta Y ) \Delta X \quad (5.9)$$

#### 5.2.4 Coefficient Multiplier

The function of the coefficient multiplier is described by the following equation

$$Y = kZ \quad (5.10)$$

This equation is written in difference form

$$\Delta Y_n + 1 = k \Delta Z_n \quad (5.11)$$

The difference form of the coefficient multiplication is not an approximation in the sense of the difference approximation of the integration, but introduces round-off error and the dynamic error. The latter error arises as the incremental output  $\Delta Y$  appears one iteration time later than the input  $\Delta Z$ .

The transfer function of the coefficient multiplier is written as

$$G(s) = \frac{Y(s)}{Z(s)} = ke^{-\tau s} \quad (5.12)$$

where  $\tau$  denotes iteration time. This approximation is inevitable because all computing elements of DAC operate in parallel and the outputs of the elements are used as inputs in the next operational period. The block diagram of the coefficient multiplier is shown in Fig. 5.6

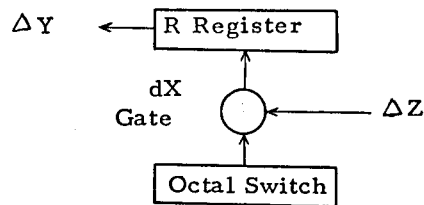


Fig. 5.6 Coefficient multiplier.

### 5.2.5 Servo Element

The role of high gain operational amplifier is filled by the servo element in DAC. The servo element accumulates the inputs  $\Delta Y_1, \Delta Y_2, \dots, \Delta Y_i$  and generates a positive signal when the content is positive and generates a negative signal when the content is negative. The operation of the servo element is represented by the following equation

$$\Delta Z_{n+1} = 2^{-N} \operatorname{sgn} \{ (Y_1 + Y_2 + \dots + Y_i) \Delta X_n \} \quad (5.13)$$

Table 5.5 shows the operation.

Table 5.5

$(Y_1 + Y_2 + \dots + Y_i) \Delta X_n$	$\Delta Z_{n+1}$
$= 0$	0
$> 0$	$2^{-N}$
$< 0$	$-2^{-N}$

### 5.2.6 Adder

The computation performed by DAC is the incremental calculus, that is both input and output of a computing element are increments from the previous states. The operation of addition is also performed on increments according to the following equation for two inputs

$$\Delta Z_{n+1} = 1/2 (\Delta Y_1 + \Delta Y_2) \Delta X_n \quad (5.14)$$

The adder is composed of an addition circuit and a R register as shown in the block diagram of Fig. 5.7.

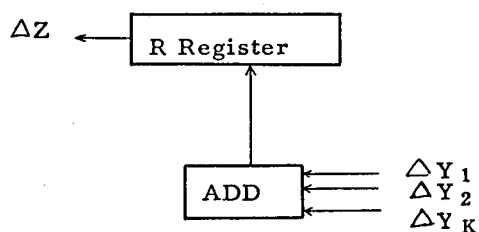


Fig. 5.7 Adder

The sum of the inputs are accumulated in R register and when the content of R register surpasses 2 a positive output is generated and the register is subtracted by 2 and when the content becomes less than -2 a negative output is generated and the register is added by 2. The operation of the adder for K inputs is described in Table 5.6

Table 5.6

$R_n + (\sum_{i=1}^K \Delta Y_i)_n$	$R_{n+1}$	$\Delta Z_{n+1}$
$\geq K$	$R_n + (\sum_{i=1}^K \Delta Y_i)_n - K$	$2^{-N}$
$\geq -K$ , and $< K$	$R_n + (\sum_{i=1}^K \Delta Y_i)_n$	0
$< -K$	$R_n + (\sum_{i=1}^K \Delta Y_i)_n + K$	$-2^{-N}$

Actually adder of many inputs is not favorable because when only one of the inputs carries signal the output of the adder appears  $K$  iteration times later.

An alternate way of composing an adder is the use of the servo-element described in the previous section. Consider one input of the three input servo element is supplied by the output of the servo element itself with the multiplication factor of two as shown in the block diagram of Fig. 5.8(a).

Referring to (5.13) the equation of operation of this circuit is written

$$\Delta Z_{n+1} = 2^{-N} \text{sgn} \{ (Y_1 + Y_2 - 2Z)_n \Delta X_n \} \quad (5.15)$$

In the steady state

$$Z = 1/2 (Y_1 + Y_2) \quad (5.16)$$

This type of adder resembles the analog adder shown in Fig. 5.8 (b)

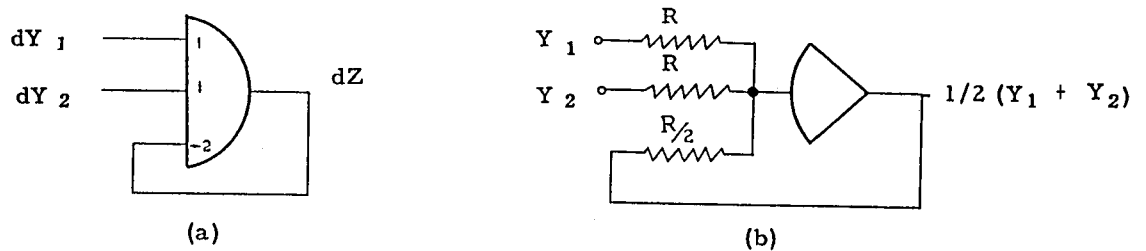


Fig. 5.8 Adder using servo element (a), and analog adder (b).

### 5.2.7 Multiplier and Divider

The operation of the multiplication

$$Z = UV \quad (5.17)$$

is transformed into the difference relation

$$\begin{aligned}\Delta Z_{n+1} &= U_n \Delta V_n + V_n \cdot \Delta U_n + \Delta U_n \Delta V_n \\ &= (U_n + \frac{1}{2} \Delta U_n) \cdot \Delta V_n + (V_n + \frac{1}{2} \Delta V_n) \cdot \Delta U_n\end{aligned}\quad (5.18)$$

which is representable by two integrators.

The division is also representable by integrators. Therefore the multiplier and the divider are not built.

#### 5.2.8 Scaling

The variables in DAC ought to be always between -1 and +1. In solving the problem on DAC, therefore, the variable should be transformed into the machine variables introducing suitable scale factors. The differential equation

$$\frac{dz}{dx} = y \quad (5.19)$$

is written in machine variables  $x$ ,  $y$  and  $z$ . They are related to  $X$ ,  $Y$  and  $Z$  by the scale factors  $\alpha$ ,  $\beta$  and  $\gamma$  as

$$X = \alpha x \quad (5.20)$$

$$Y = \beta y \quad (5.21)$$

$$Z = \gamma z \quad (5.22)$$

when  $X$  is the independent variable of the original differential equation  $\alpha$  is determined from the required computation speed and  $\beta$  and  $\gamma$  are determined from the following inequality.

$$\beta |Y|_{\max} < 1, \quad \gamma |Z|_{\max} < 1 \quad (5.23)$$

The machine equation for Eq. (5.19) is then

$$\frac{dZ}{dX} = \frac{\gamma}{\alpha \beta} Y \cdot dX \quad (5.24)$$

It is favorable to determine the scale factors as

$$\frac{\gamma}{\alpha \beta} = 2^k \quad (5.25)$$

where  $k$  is an integer. Then (5.24) reduces to

$$dZ = 2^k Y \cdot dX \quad (5.26)$$



which is executable by the integrater changing the effective length of the Y register.

### 5.3 Logical Design

#### 5.3.1 Number System

In this section the logical construction of the computing element of DAC is described.

As has been described in the previous section the operation of the elements of DAC is based on incremental calculus and the signals emitted or introduced are always incremental signal of which magnitude is either 0,  $+2^{-N}$  or  $-2^{-N}$ . These signals are transmitted by a pair of wires one of which is named positive line and the other negative line. When a signal is carried on the positive line the output is  $2^{-N}$ , when a signal is on the negative line the output is  $-2^{-N}$ , and when neither of the lines carry signal the output is zero. The signal never appears on both wires simultaneously.

The signal on these wires is represented by the non-return-to-zero system which holds the state for an iteration time beginning from P1 and ending at P20. The maximum frequency of this incremental signal is 5 kc while signals inside the computing elements are 100 kc. The time chart is shown in Fig. 5.9.

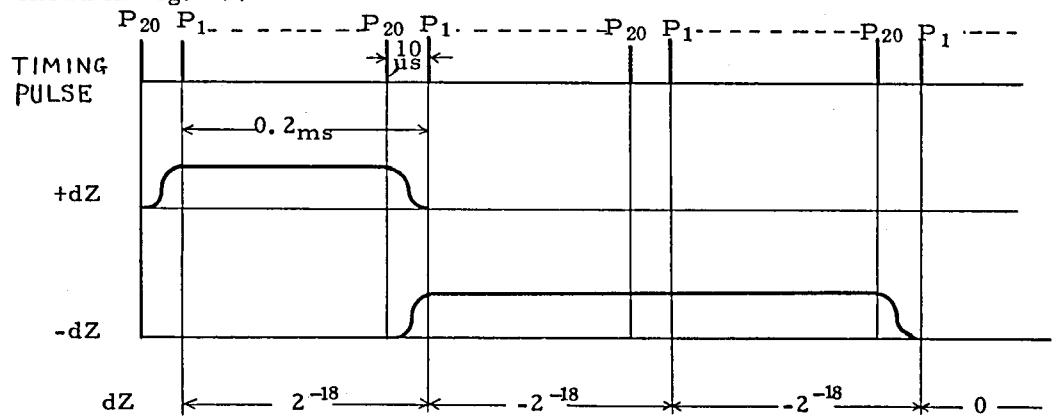


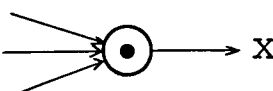
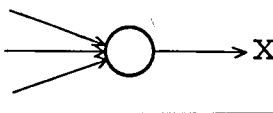
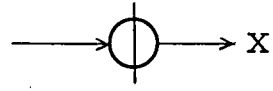
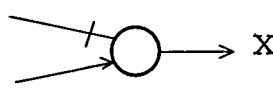
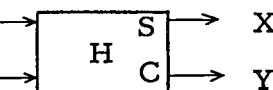
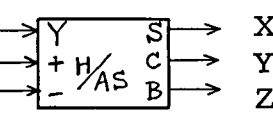

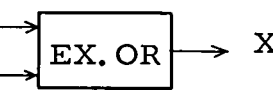
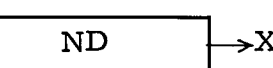
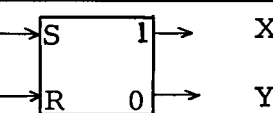
Fig. 5.9 Time chart showing timing pulse and output signals of computer elements.

#### 5.3.2 Gate Circuits

The gate circuits used in DAC are shown in Table 5.7.

Table 5.7

Symbols of gate circuits of DAC.

No.	Gate Circuit	Symbol	Logical Equation
1	AND GATE		$X = A \cdot B \cdot C$
2	OR GATE		$X = A + B + C$
3	NOT GATE		$X = \bar{A}$
4	INHIBIT GATE		$X = \bar{A} \cdot B$
5	HALF ADDER		$X = \bar{A} \cdot B + A \cdot \bar{B}$ $Y = A \cdot B$
6	HALF ADDER-SUBTRACTOR		$X = \bar{A} \cdot (B + C) + A \cdot (\bar{B} + \bar{C})$ $Y = A \cdot B$ $Z = \bar{A} \cdot C$
7	COMPLEMENTER		$X = A'$
8	EXCLUSIVELY-OR		$X = \bar{A} \cdot B + A \cdot \bar{B}$
9	DELAY		$X_n + N = A_n \cdot X$
10	FLIP-FLOP		$X_n + 1 = A_n \cdot \bar{X}_n + \bar{B}_n \cdot X_n$ $Y_n + 1 = \bar{A}_n \cdot Y_n + B_n \cdot Y_n$ $X_n = \bar{Y}_n$

The operation of the flip-flop in the sixth column is so defined that the output maintains its previous state when the input signal is absent, output of "1" becomes 1 and output of "0" becomes 0 when an input signal is applied at "S" input and "1" output becomes 0 and "0" output becomes 1 when a signal is applied at "R" input. When signals are applied at both input terminals the output of the flip-flop reverses its previous state. The logical equation of this flip-flop is then written as follows.

$$\begin{aligned} X_{n+1} &= \bar{X}_n \cdot Y_n \cdot A_n \cdot \bar{B}_n + \bar{X}_n \cdot Y_n \cdot A_n \cdot B_n + X_n \cdot \bar{Y}_n \cdot \bar{A}_n \cdot \bar{B}_n + X_n \cdot \bar{Y}_n \cdot A_n \cdot \bar{B}_n \\ &= \bar{B}_n \cdot X_n + A_n \cdot \bar{X}_n \end{aligned} \quad (5.27)$$

$$\begin{aligned} Y_{n+1} &= \bar{X}_n \cdot Y_n \cdot \bar{A}_n \cdot B_n + X_n \cdot Y_n \cdot \bar{A}_n \cdot B_n + X_n \cdot \bar{Y}_n \cdot \bar{A}_n \cdot B_n + X_n \cdot \bar{Y}_n \cdot A_n \cdot B_n \\ &= \bar{A}_n \cdot Y_n + B_n \cdot \bar{Y}_n \end{aligned} \quad (5.28)$$

Other gate-circuits of Table 5.7 need no particular explanation.

### 5.3.3 R Register

R register used in integrater and coefficient multiplier is a twenty bits accumulator accumulating the output of Y register or corresponding quantity. When its content becomes larger than one or becomes negative a positive or negative signal is generated. The operation of R register is as described by Table 5.3. The second case of the table is an overflow and the third case is a underflow. The detection of the overflow and the underflow is done by inspection of the sign of  $Y_n$  and  $R_n + Y_n$  because  $R_n$  is non-negative. When  $R_n + Y_n$  is negative while  $Y_n$  is positive overflow took place and when  $R_n + Y_n$  is negative and  $Y_n$  is negative underflow took place.

This is shown in Table 5.8

Table 5.8

**Truth table of output circuit of R Register.**

case	sgn $Y_n$	sgn $(R_n + Y_n)$	$\Delta Z_{n+1}$
1	+	+	0
2	+	-	+
3	-	+	0
4	-	-	-

Denoting the sign bit of  $Y_n$  by  $A$  and that of  $R_n + Y_n$  by  $B$  the following logical relations hold.

$$\text{Overflow} = \overline{A} \cdot B \quad (5.29)$$

$$\text{Underflow} = A \cdot B \quad (5.30)$$

After overflow or underflow are detected the sign bit of  $R_n + Y_n$  is erased to perform the operation specified by Table 5.3. As  $\Delta Z$ , the output of R register should maintain the signal for an iteration time the overflow and underflow signals are used to set flip-flops of which "1" outputs are connected to the positive line and the negative line respectively. These flip-flops are reset by P20. Fig. 5.10 shows the logical circuit of the R register.

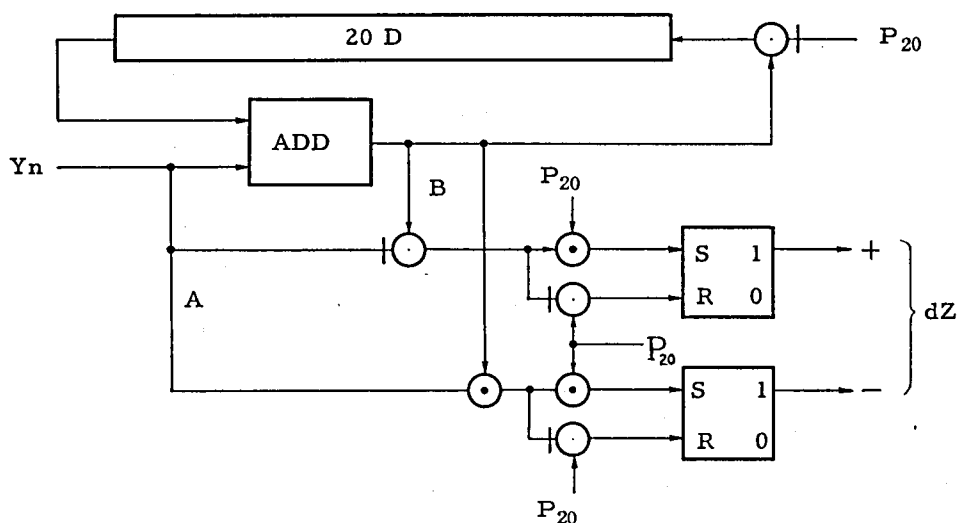


Fig. 5.10 Logical circuit of R register

### 5.3.4 Y Register

Y register of the integrater is also a twenty bits accummulator but

differs from R register in its operation. The input signal to Y register is either one of  $2^{-18+k}$ ,  $-2^{-18+k}$  or 0.  $k$  is fixed during the operation but may be changed from 0 to 17 depending on the scale factor. To change  $k$  the input signal is strobed by either one of the timing pulses of P2, P3, ..., P9. As the magnitude of  $Y_n$  is limited as

$$-1 < Y_n \leq 1 \quad (5.31)$$

the overflow or underflow from Y register is detected for alarm. The logical equation of this alarm circuit is given by

$$X = \bar{A} \cdot B \cdot C \cdot \bar{D} + A \cdot \bar{B} \cdot \bar{C} \cdot D \quad (5.32)$$

where

- A : sign bit of  $Y_n$
- B : sign bit of  $Y_n + \Delta Y_n$
- C : + dY
- D : - dY
- X : Overflow

Another component of Y register is the  $\Delta Y$  register the operation of which is described in Table 5.4.

Y register is a two-bits reversible counter as shown in Fig. 5.11

In Fig. 5.12 logical circuit of the Y register is shown.

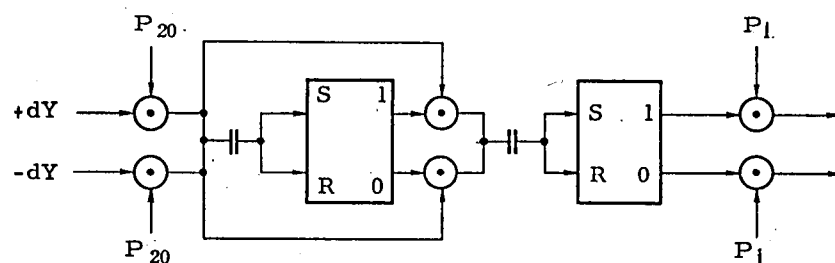


Fig. 5.11  $\Delta Y$  register

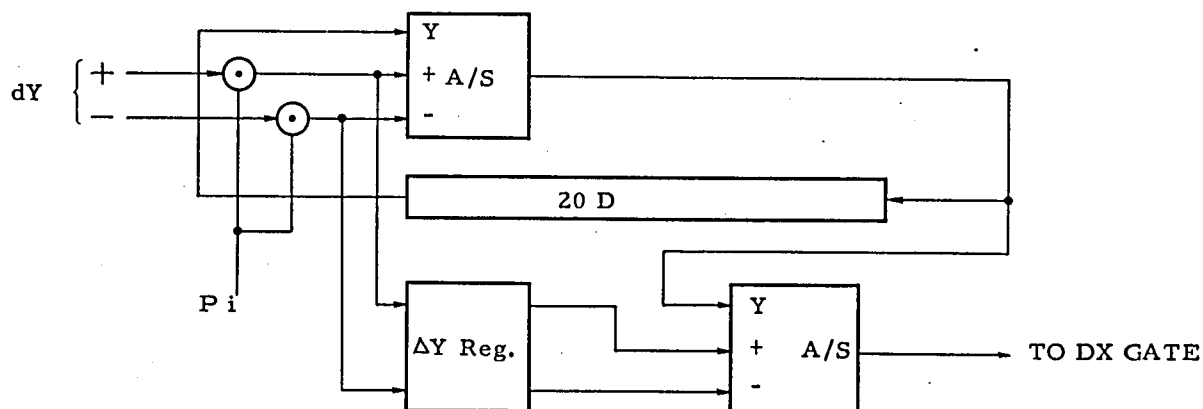


Fig. 5.12 Logical circuit of Y register

### 5.3.5 Integrater

The integrater is composed of R register, Y register and dX gate. dX gate controls the signal sent from Y register in a way that input signal to R register changes its sign when dX is negative. The logical circuit of dX gate is shown in Fig. 5.13

Before beginning the computation the initial values are loaded in Y register of all integraters. Initial value of  $2^{-1}$  is also introduced in the R register to eliminate the offset error.

The content of Y register is cleared before the operation by the preset pulse which is generated for an iteration time by the press of a push-button on control panel. At the same time initial value set on the octal switch is introduced by this preset pulse into the Y register. The computation begins after the preset pulse disappears. Time chart of Fig. 5.14 shows the sequence of this operation. Into R register P19 is introduced by the preset pulse. The octal switch for setting the initial value is identical to that used in coefficient multiplier which will be described later. The logical circuit of the complete integrater is shown in Fig. 5.14

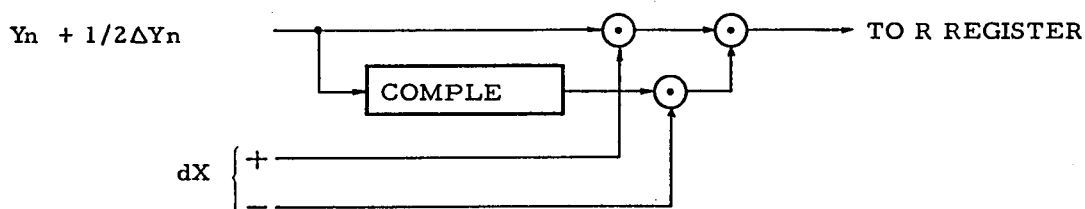


Fig. 5.13 Logical circuit of dX gate

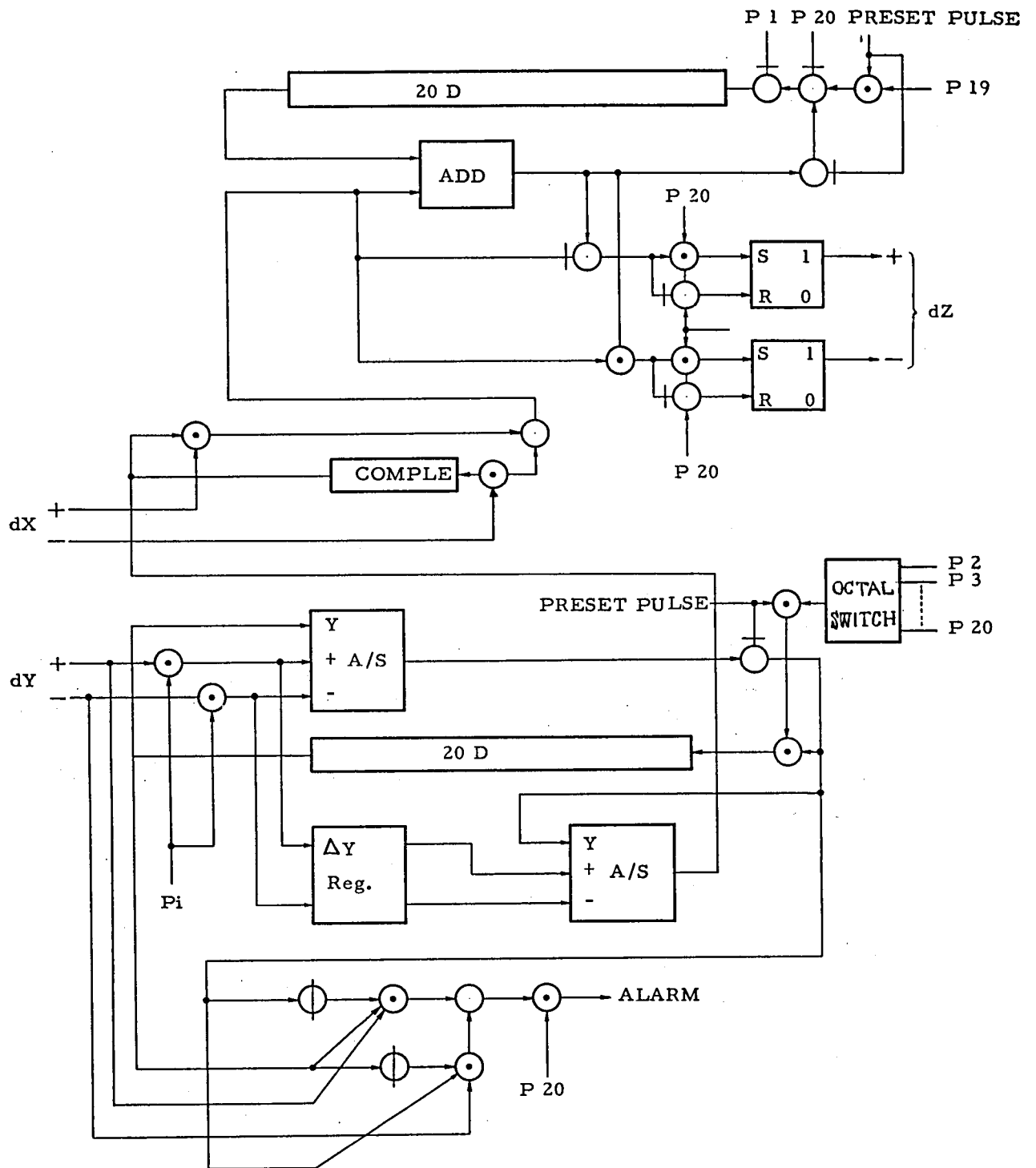


Fig. 5.14 Logical circuit of the integrater

### 5.3.6 Coefficient Multiplier

The coefficient Multiplier generates output  $\Delta Y$  subject to the input  $\Delta Z$  by the following relation.

$$\Delta Y_{n+1} = k \Delta Z_n \quad (|k| < 1) \quad (5.33)$$

The circuit of the coefficient multiplier is similar to the integrater except Y register of integrater is replaced by the coefficient switch. The coefficient switch is a six digits octal switch shown in Fig. 5.15.

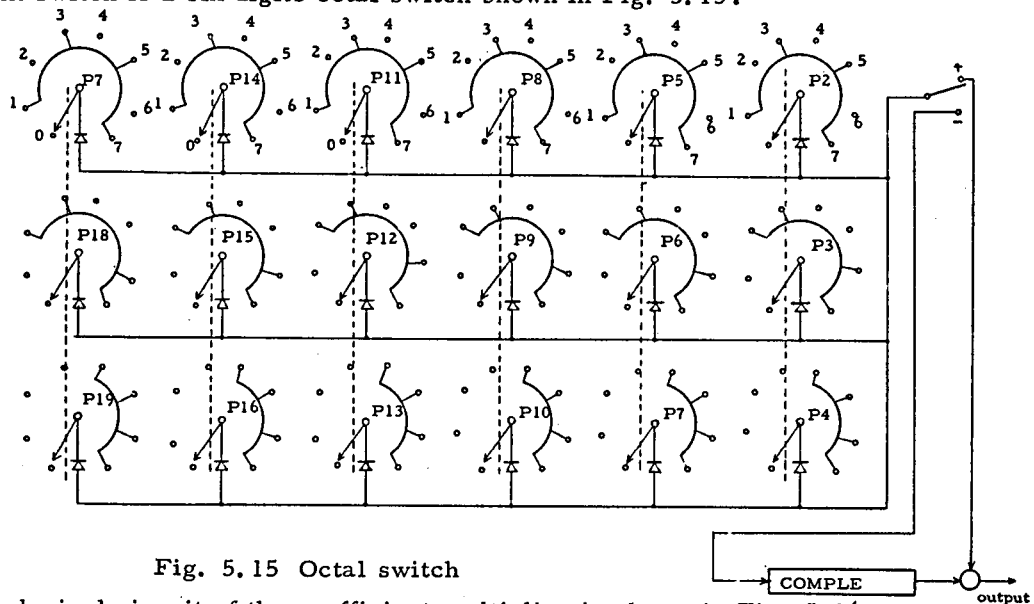


Fig. 5.15 Octal switch

The logical circuit of the coefficient multiplier is shown in Fig. 5.16.

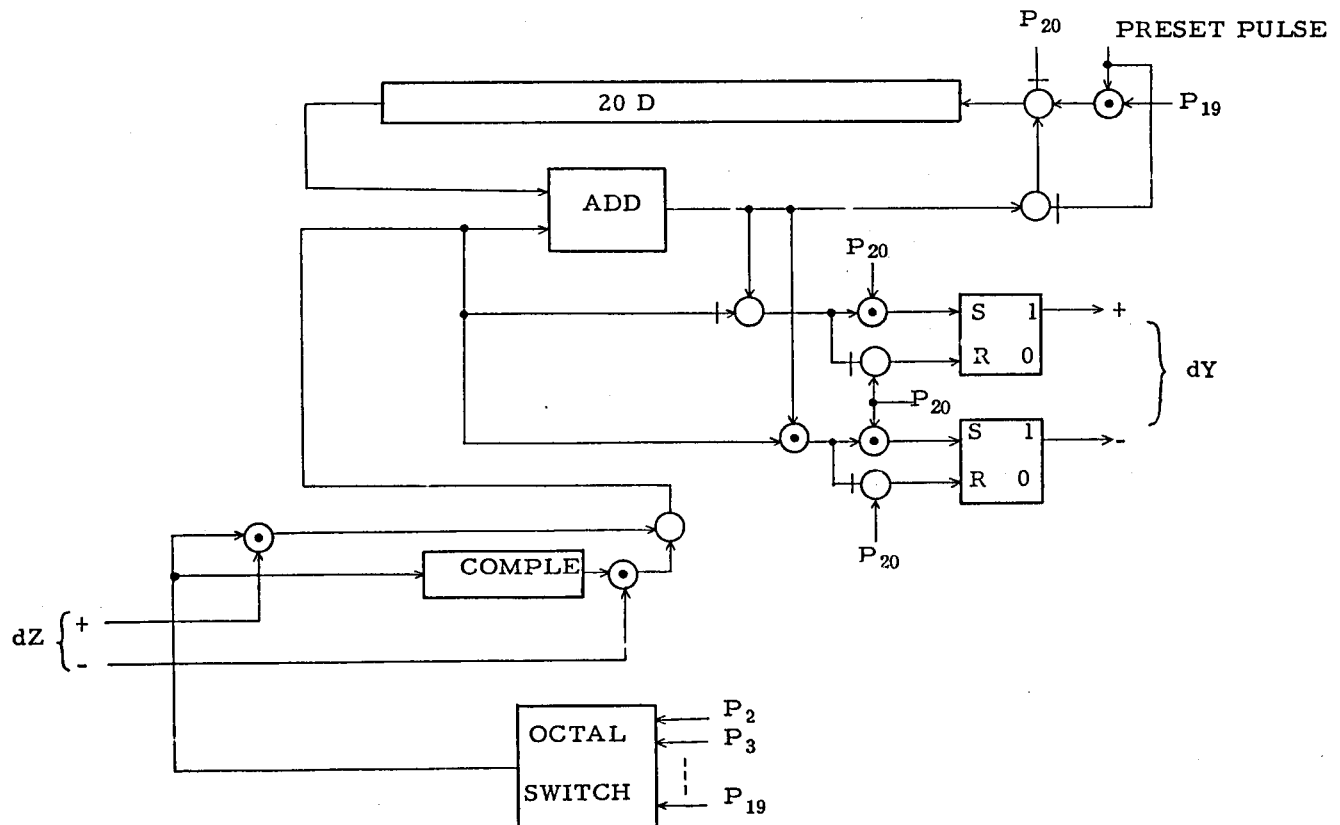


Fig. 5.16 Logical circuit of coefficient multiplier



### 5.3.7 Servo Element

The Y register of the servo element is different from that of the integrater as the input to the register is more than one. The addition of more than three numbers may be executed by cascading adder-subtracters.

The output circuit is a pair of flip-flops which are set depending on the sign of the content of Y register. The logical equations of the output circuit of the servo element is as follow.

$$X = \bar{A} \cdot B \cdot \bar{C} + A \cdot \bar{B} \cdot C = \bar{A} \cdot B + A \cdot C \quad (5.34)$$

$$Y = \bar{A} \cdot \bar{B} \cdot C + A \cdot B \cdot \bar{C} = A \cdot B + \bar{A} \cdot C \quad (5.35)$$

where

A : sign bit of  $\sum Y_i$

B :  $+\Delta X_n$

C :  $-\Delta X_n$

X :  $+\Delta Z_{n+1}$

Y :  $-\Delta Z_{n+1}$

The complete logical circuit of the servo element is shown in Fig. 5.17.

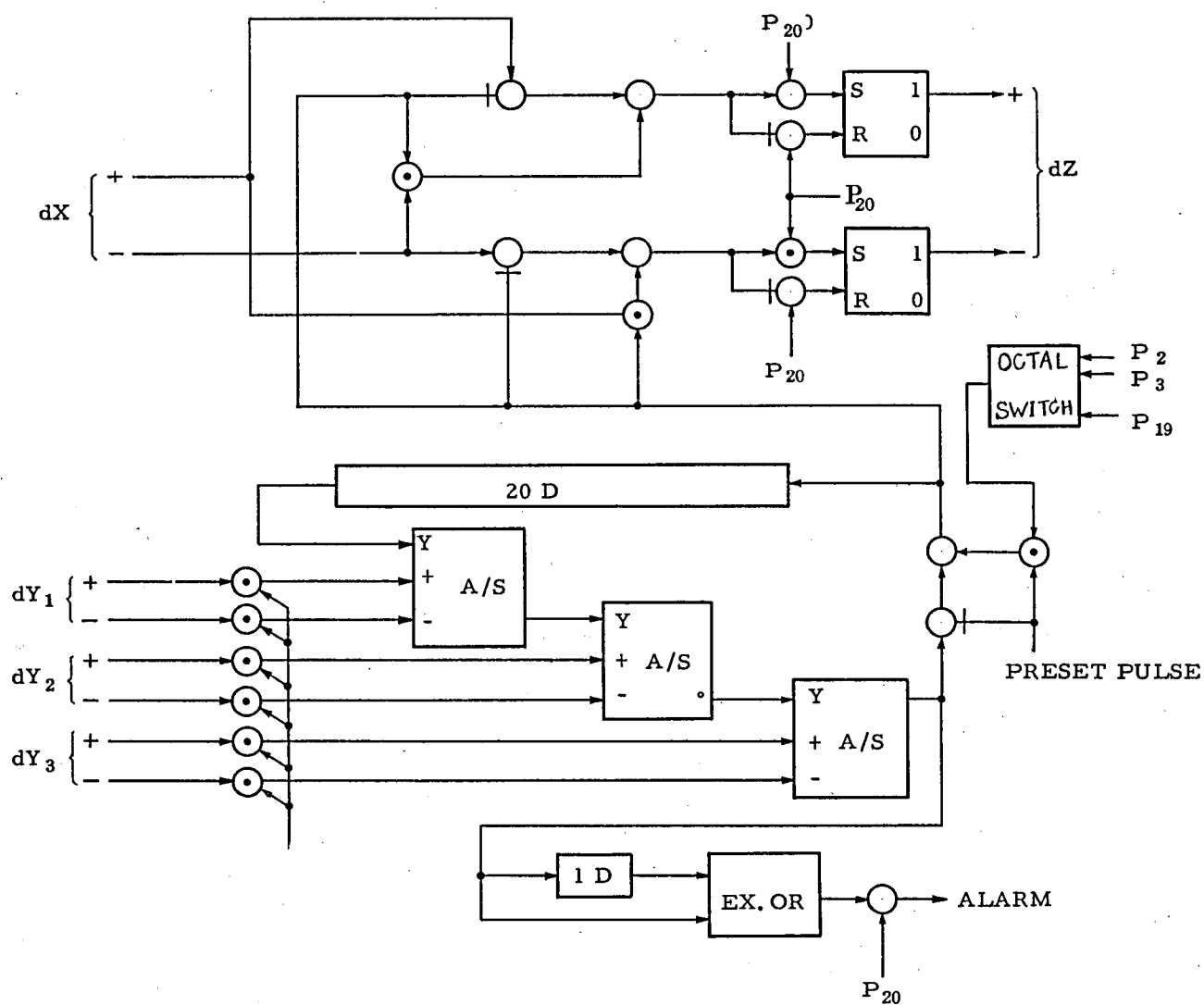


Fig. 5.17 Logical circuit of servo element

### 5.3.8 Adder

The logical circuit of the adder is similar to the R register of the integrater except the input is more than one. The output circuit similar to R register needs sign bit of  $(\Delta Y_1 + \Delta Y_2)$ . This is represented by the following logical equation.

$$\begin{aligned} X &= \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot D + A \cdot \bar{B} \cdot C \cdot D + A \cdot \bar{B} \cdot C \cdot \bar{D} \\ &= \bar{A} \cdot D + B \cdot \bar{C} \end{aligned} \quad (5.36)$$

where  $A = +\Delta Y_1$ ,  $B = -\Delta Y_1$ ,  $C = +\Delta Y_2$ , and  $D = -\Delta Y_2$ .

The complete logical circuit of the adder for two inputs is shown in Fig. 5.18.

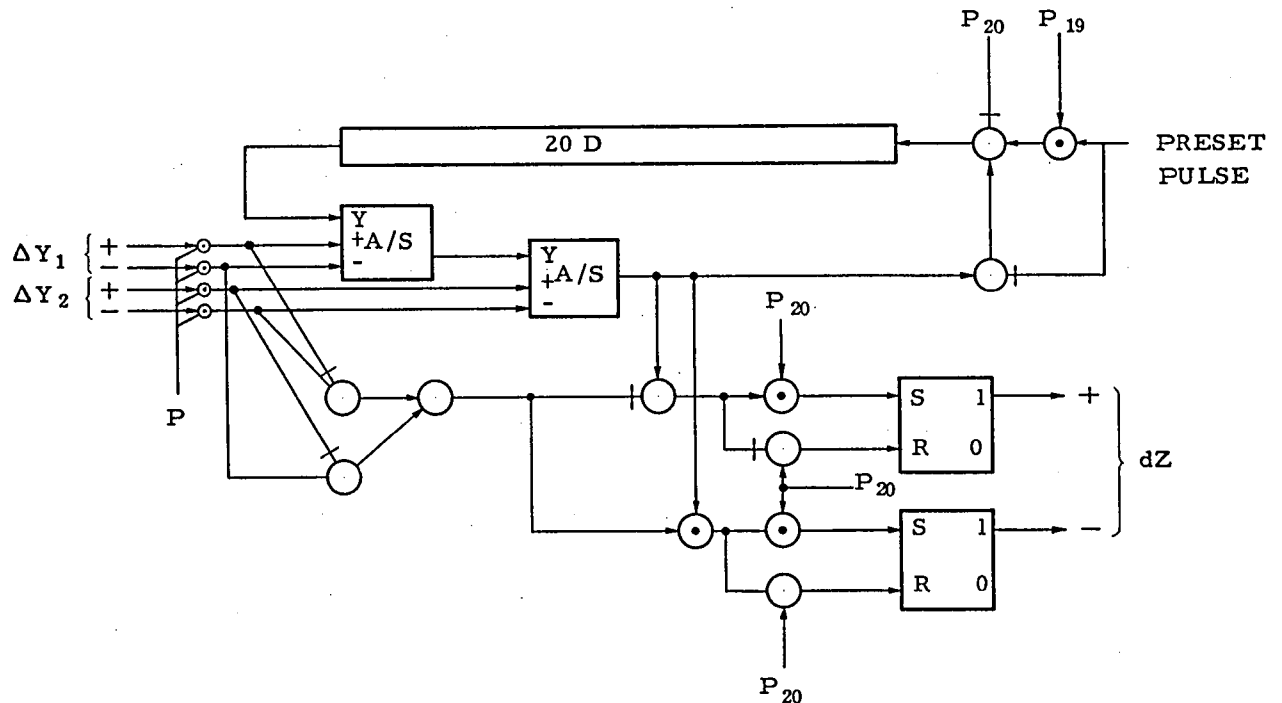


Fig. 5.18      Logical circuit of adder

The register 20 D in this logical circuit need not be a twenty-bits shift register but is sufficient to be two-bits shift register storing sign bit and a number bit.

#### 5.4 Model Computer DAC - 1 74)

For the purpose of testing the logical <sup>design</sup> and the feasibility of DAC a small-sized model computer DAC-1 is built. Fig 5.19 shows DAC-1 and Table 5.9 shows the components of DAC-1 and their specifications.

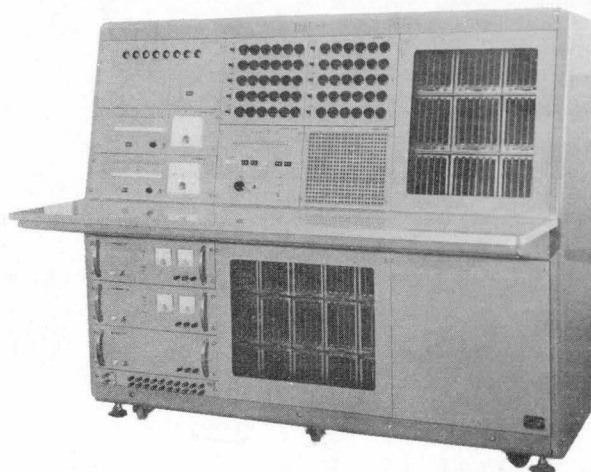


Fig. 5.19 Model computer DAC - 1

Table 5.9

Components	Q'ty	Specifications
1 integrater	5	trapezoidal formula
2 coefficient multiplier	2	
3 servo element	3	three inputs
4 D-A converter	2	10 bits - 10 - 10 V
5 octal switch	10	6 octal digits
6 clock pulse generater	1	100 kc, 1 c/s, manual
7 timing pulse generater	1	P1, P2, . . . . . , P20
8 indicator	1	20 bits
9 connecting board	1	432 points
10 step counter	1	maximum $10^8$ steps
11 control panel	1	timing pulse start-stop sw. computation start-stop sw.

As the function of the computing elements were described in the previous sections the operation of the control circuit of DAC - 1 will be described in this section.

The block diagram of the shift pulse generator is shown in Fig. 5.20

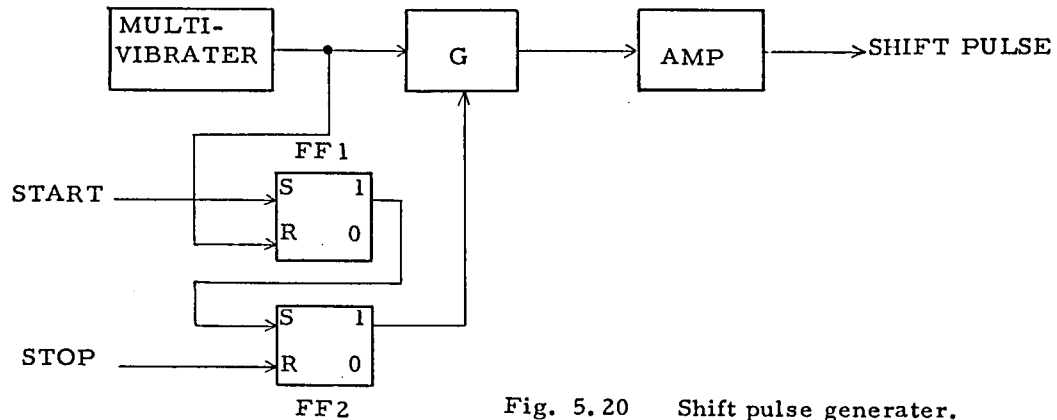


Fig. 5.20 Shift pulse generator.

When power switch is thrown in the multivibrator begins to oscillate and the flip-flop FF1 is reset. When start pulse is sent from the computation start switch it sets FF1 and then FF2 and opens gate G. The pulses from the multivibrator is then sent to the amplifier and the shift pulse is obtained.

The timing pulses P1, P2....., P20 are generated by 20-bits shift register. After the shift pulse <sup>is</sup> generated the timing pulses are generated by the timing pulse start switch. The timing pulses appear from P1. The logical circuit of the timing pulse generator is shown in Fig. 5.21.

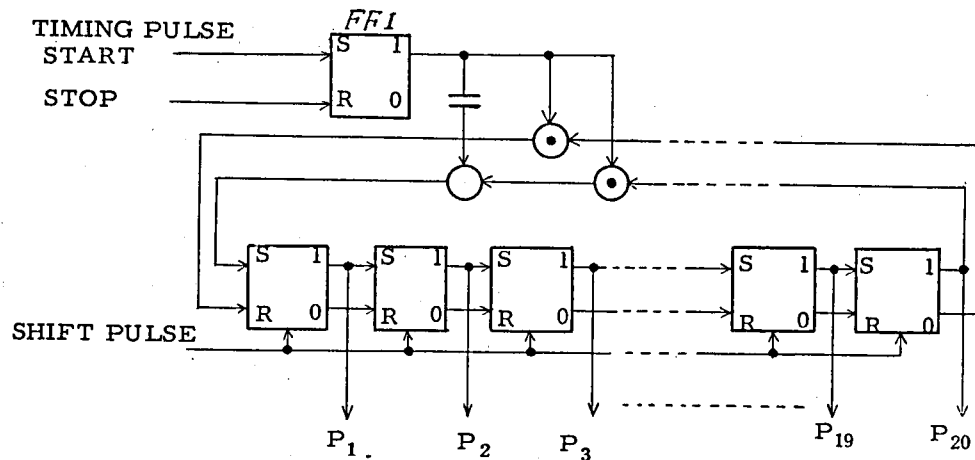


Fig. 5.21 Timing pulse generator.

By the timing-pulse-start-signal the flip-flop FF1 is set and gates are open completing the loop of the ring counter. At this moment the first flip-flop of the ring counter is set by a pulse sent from FF1 through differentiating capacitor. Thereafter this one bit circulates in the ring counter generating timing pulses  $P_1, P_2, \dots, P_{20}$  as it passes each flip-flop.

The indicator is built to monitor the contents of the registers. This is again a 20-bits shift register with neon tube indicator attached to each stage of the register. By sending an "indicate" pulse by the "indicate" switch during the operation of DAC the content of a register to which the indicator is connected through selector switch is sent into the shift register of the indicator. When the "indicate" pulse is sent again the previous result is replaced by the new content. Fig. 5.22 gives the logical circuit of the indicator.

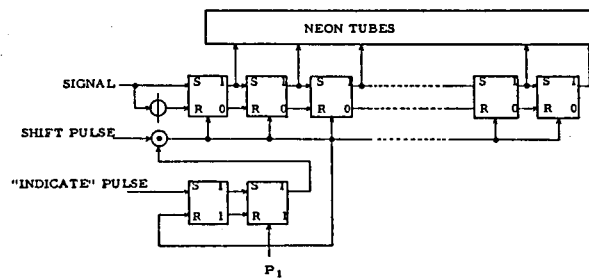


Fig. 5.22 Logical circuit of the indicator

For loading initial values in Y registers of the integrators and the servo elements and  $2^{-1}$  in R registers preset pulse P is used. The preset pulse is generated at the beginning of computation and lasts only for an iteration time. The logical circuit of the preset pulse generator is given in Fig. 5.23.

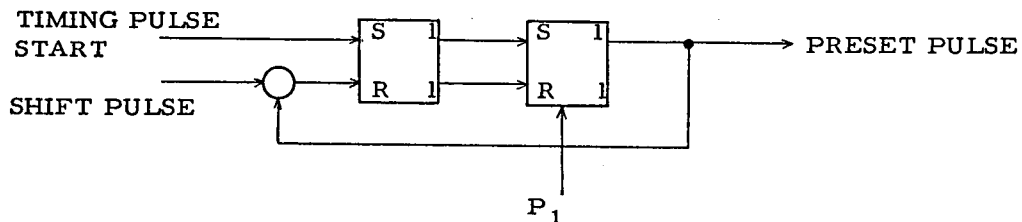


Fig. 5.23 Preset pulse generator

Fig. 5. 24

DAC solution of the first order differential equation :

$$\frac{dY}{dX} + 2^K Y = 0$$

$$X=0, Y=1.$$

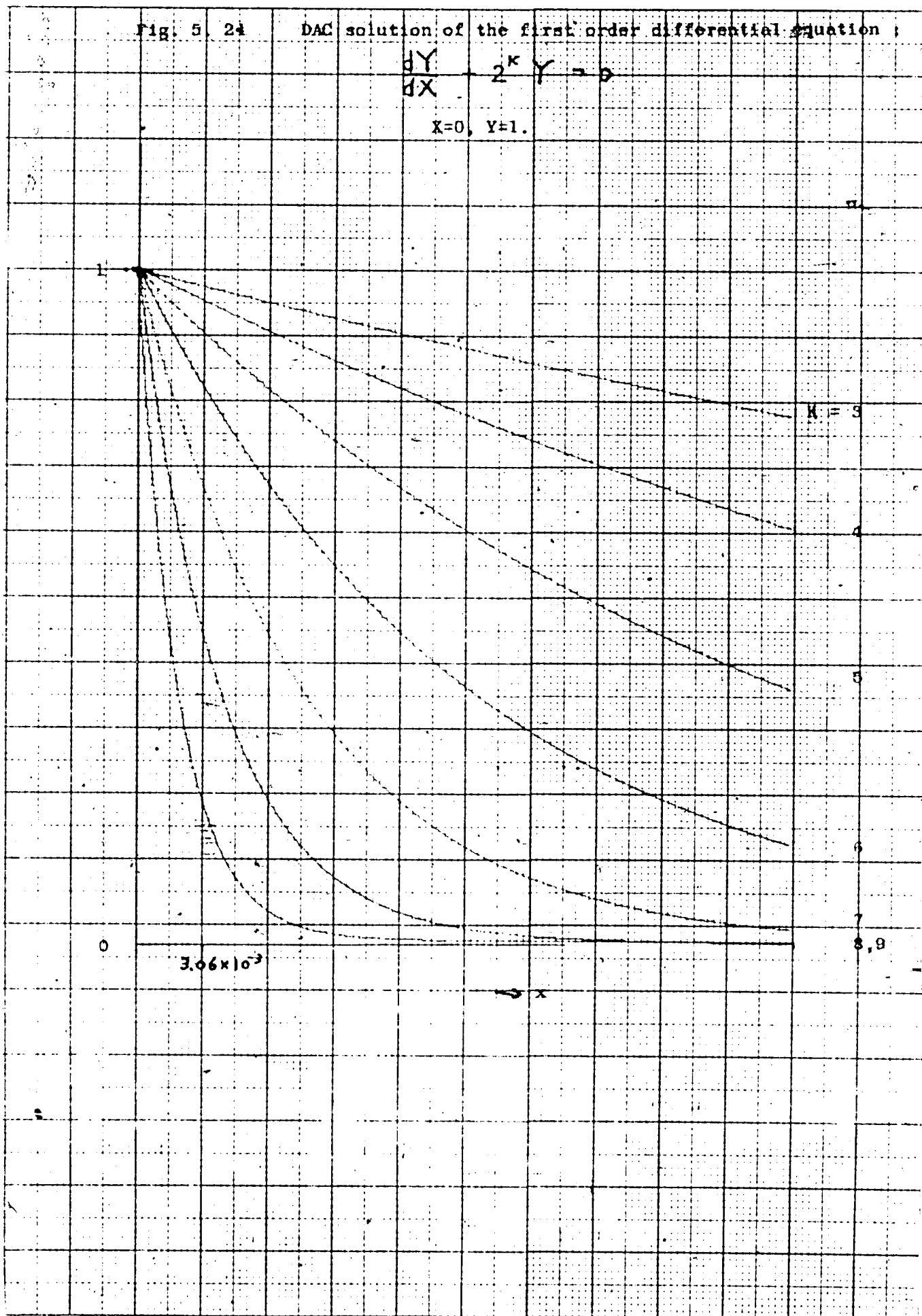


Fig. 5.24 DAC solution of the first order differential equation:

$$\frac{dY}{dX} + 2K_Y = 0$$

$$X=0, Y=1.$$

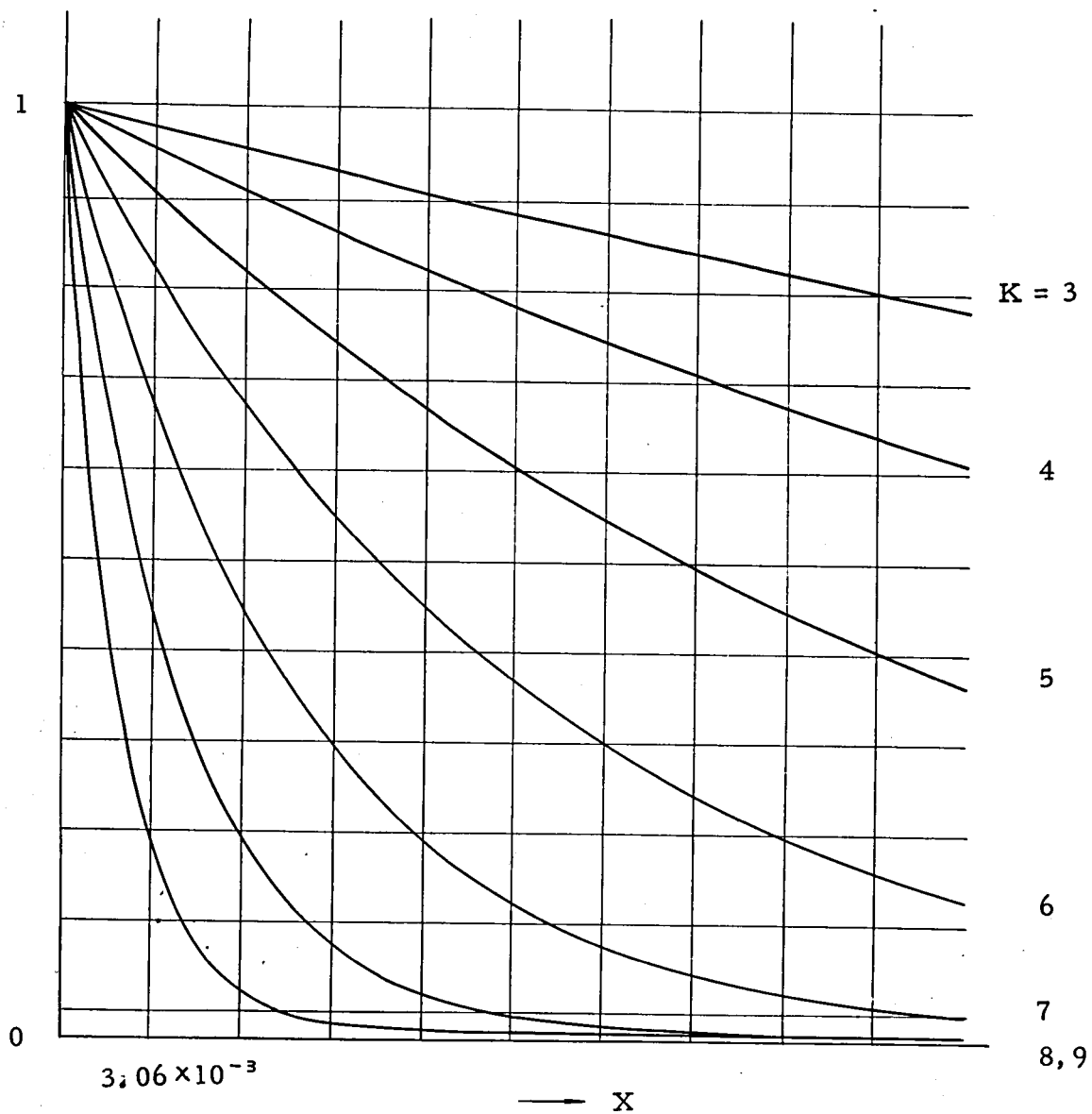




Fig. 5.25 DAC solution of the second order differential equation:

$$\frac{d^2 Y}{d X^2} + 2^{2K} Y = 0, \quad X=0, Y=1, Y'=0.$$

by the Euler integrators.

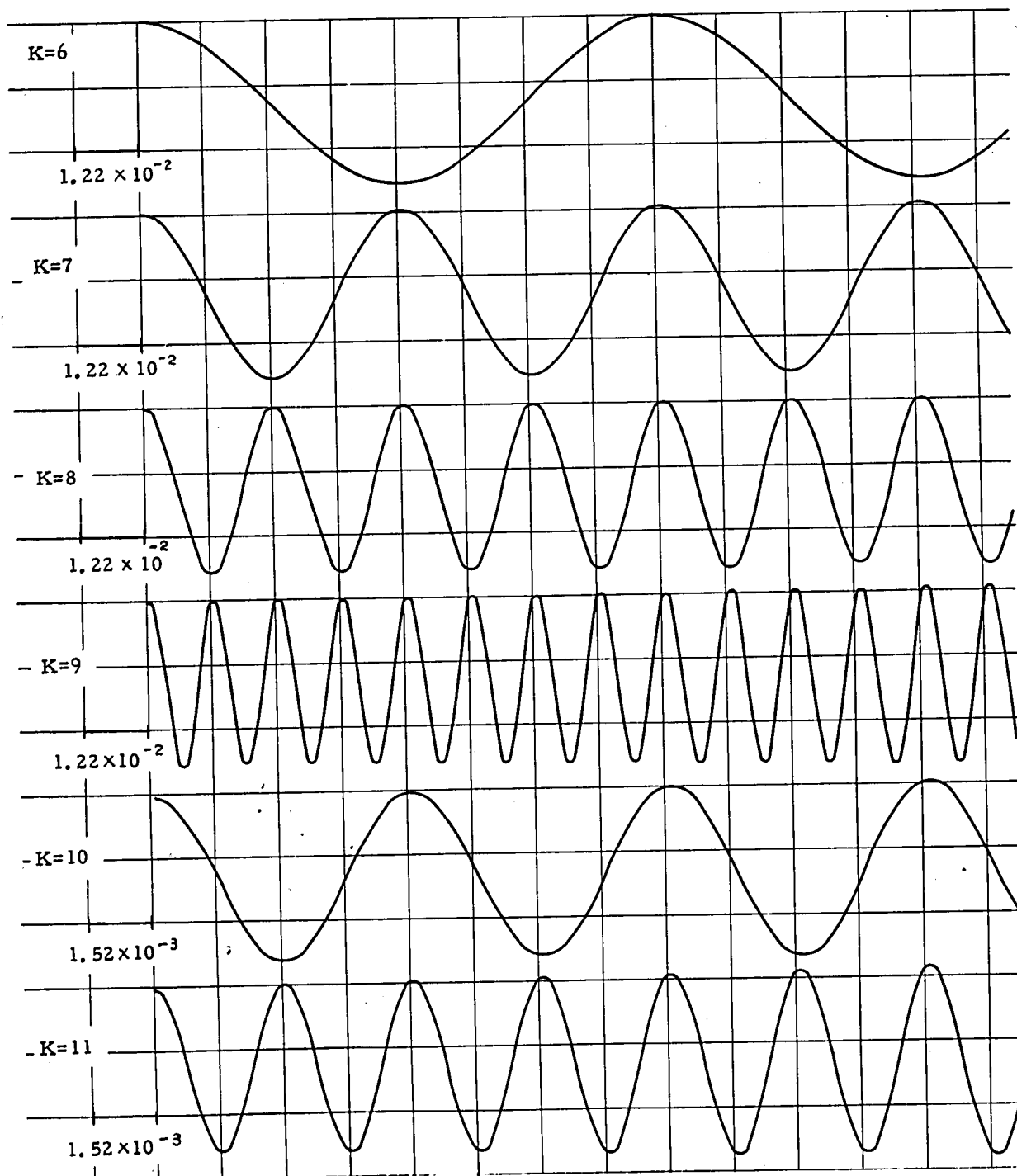


Fig. 5. 25 DAC solution of the second order differential equation :

$$\frac{d^2 Y}{dX^2} + 2^{2K} Y = 0, \quad X=0, Y=1, Y'=0.$$

by the Euler integrators.

K=6

$1.22 \times 10^{-2}$

K=7

$1.22 \times 10^{-2}$

K=8

$1.22 \times 10^{-3}$

K=9

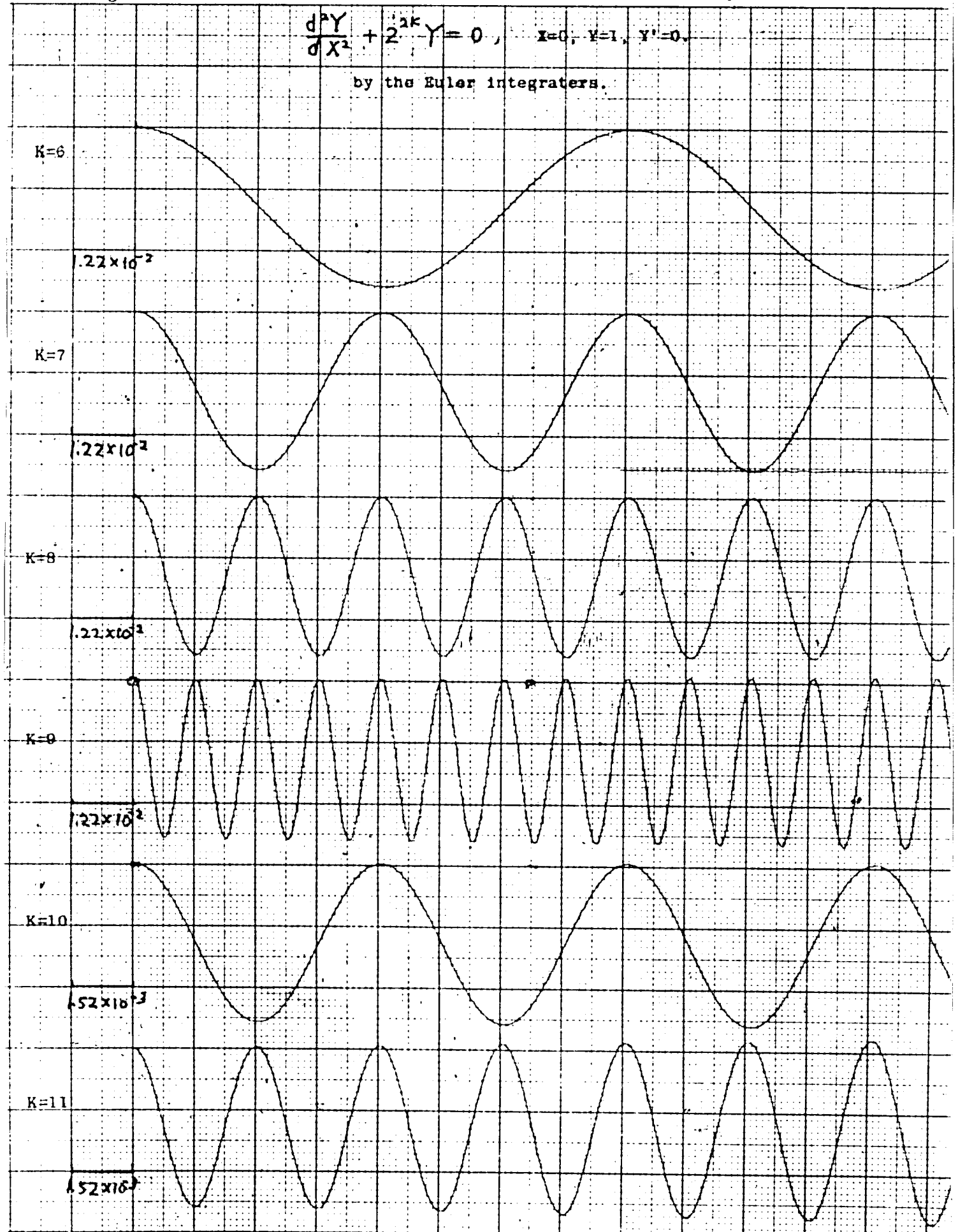
$1.22 \times 10^{-2}$

K=10

$1.52 \times 10^{-3}$

K=11

$1.52 \times 10^{-3}$



The result of computation of DAC - 1 is converted into analog voltage by the digital - to - analog converter and is recorded by the pen oscillograph. dZ pulses from the computing elements are counted by reversible binary counter to which a weight circuit is connected.

Examples of calculation by DAC - 1 are shown. The first example is the following equation.

$$\frac{dZ}{dX} + Z = 0 \quad (5.37)$$

$$X = 0, \quad Z = Z_0 \quad (5.38)$$

The results of computation for different initial values are shown in Fig. 5.24.

The error of this computation is discussed in later section.

As a next example the next differential equation is solved by DAC-1.

$$\frac{d^2Z}{dX^2} + 2^{2k}Z = 0 \quad (5.39)$$

$$X = 0, \quad Z = 0.400000 \quad (8), \quad \frac{dZ}{dX} = 0 \quad (5.40)$$

The results of computations for different values of k are shown in Fig. 5.25.

Let one iteration time be  $\tau_0$  the relation between X and the real time t (sec.) is

$$t = 2^{18} \tau_0 X \text{ (seconds)} \quad (5.41)$$

and eq. (5.39) is rewritten as

$$\frac{d^2Z}{dt^2} + \left( \frac{2^{K-18}}{\tau_0} \right) \cdot Z = 0 \quad (5.42)$$

The frequency of the solution of eq. (5.37) is <sup>then</sup> the

$$f(k) = \frac{1}{2\pi} \cdot \frac{2^{k-18}}{\tau_0} \quad (5.43)$$

As  $\tau_0 = 2 \times 10^{-4}$  seconds f(k) is

$$f(k) = 0.003 \times 2^k \text{ c/s} \quad (5.44)$$

Table 5.10 gives f(k) for different values of k.

As will be readily understood for k larger than 14 is unpractical because the solutions represented by less than four bits are too inaccurate. In Fig.

5.25 solutions for k = 6, 8, 9, 10, ~~11, 12, 13, 14~~ and 15 are shown.

7,

Fig. 5. 26 DAC solution of the second order differential equation :

$$\frac{d^2 Y}{dX^2} + 2^{10} Y = 0$$

on the phase plane.

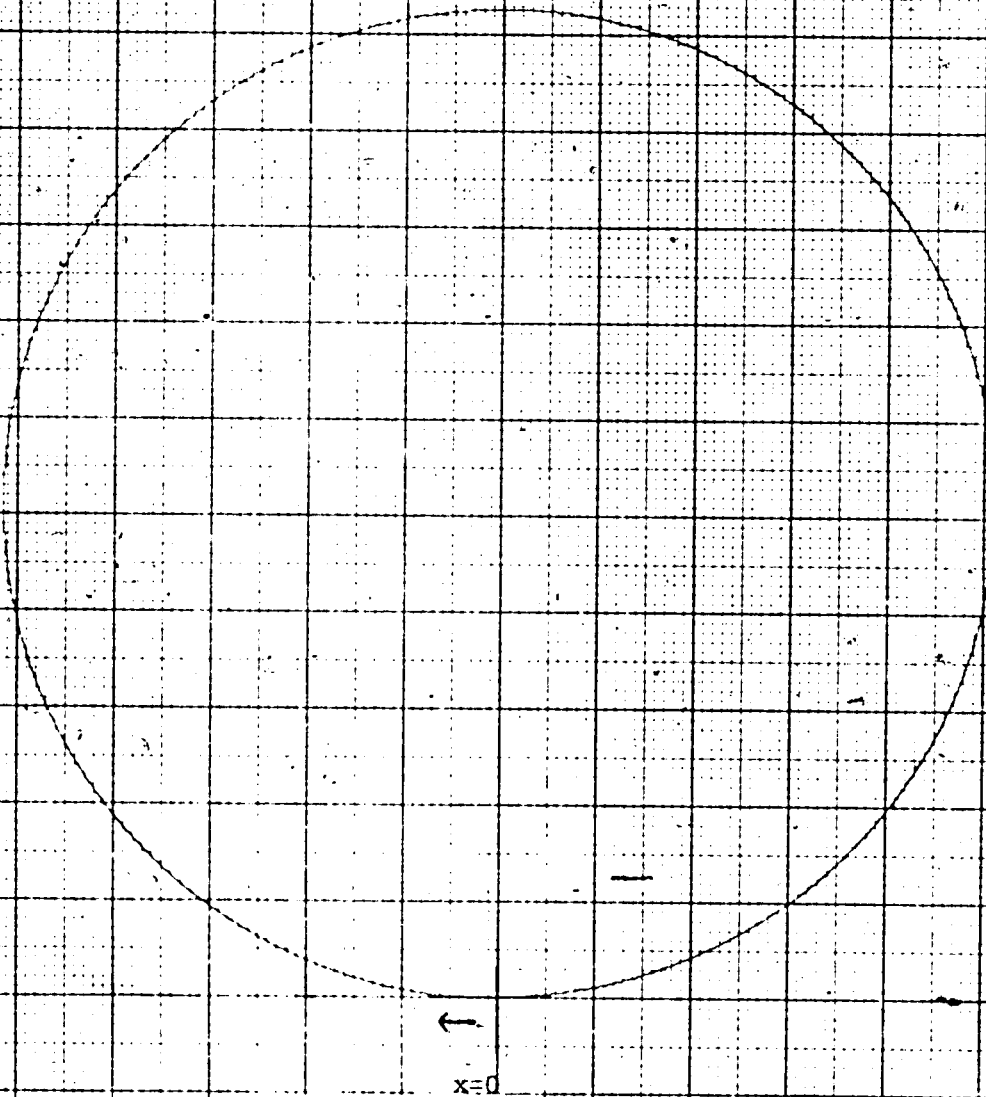


Fig. 5. 26 DAC solution of the second order differential equation:

$$\frac{d^2 Y}{d X^2} + 2^{10} Y = 0$$

on the phase plane.

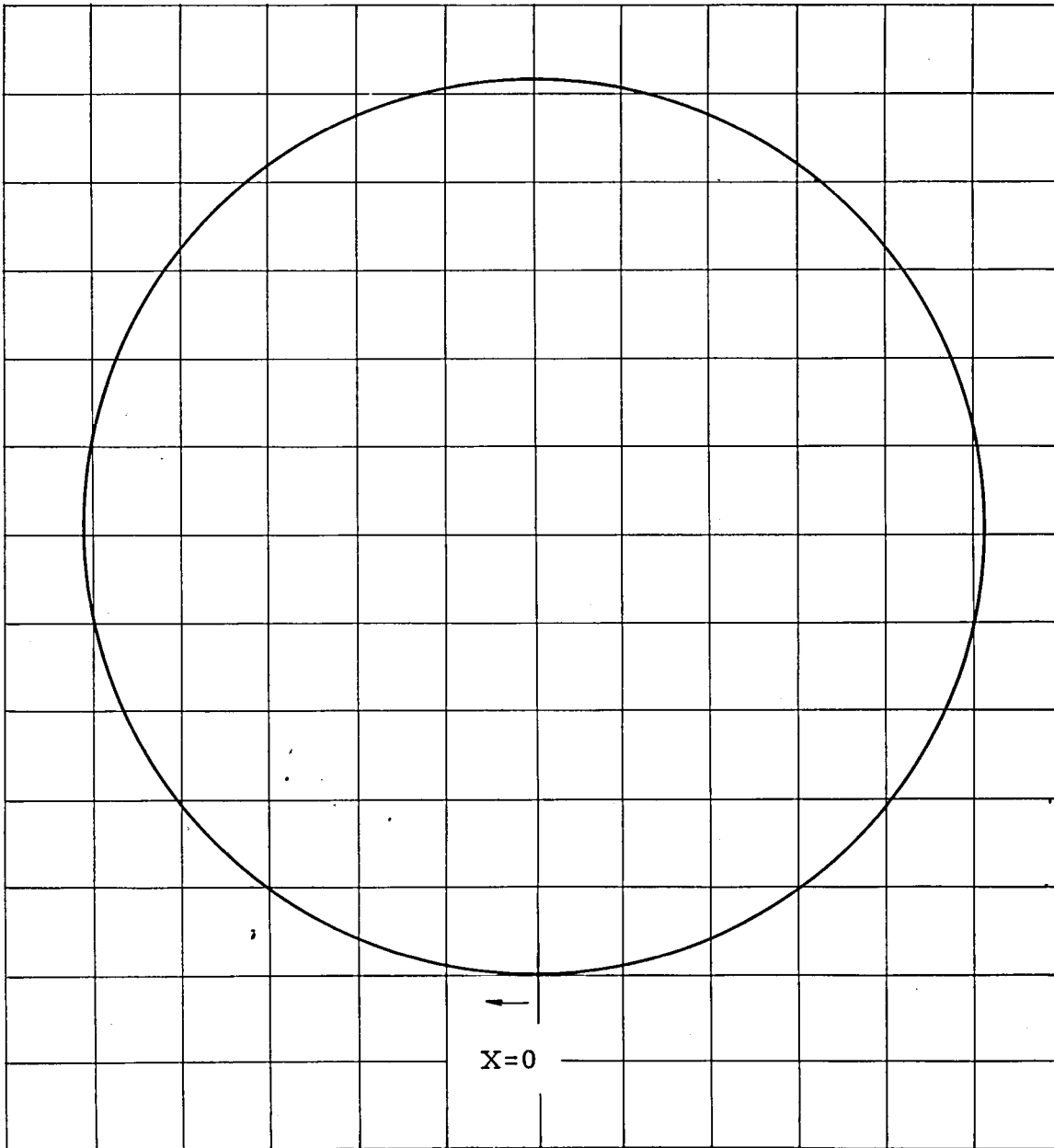


Fig. 5. 27 DAC solution of the first order differential equation:

$$\frac{dY}{dX} - X = 0$$

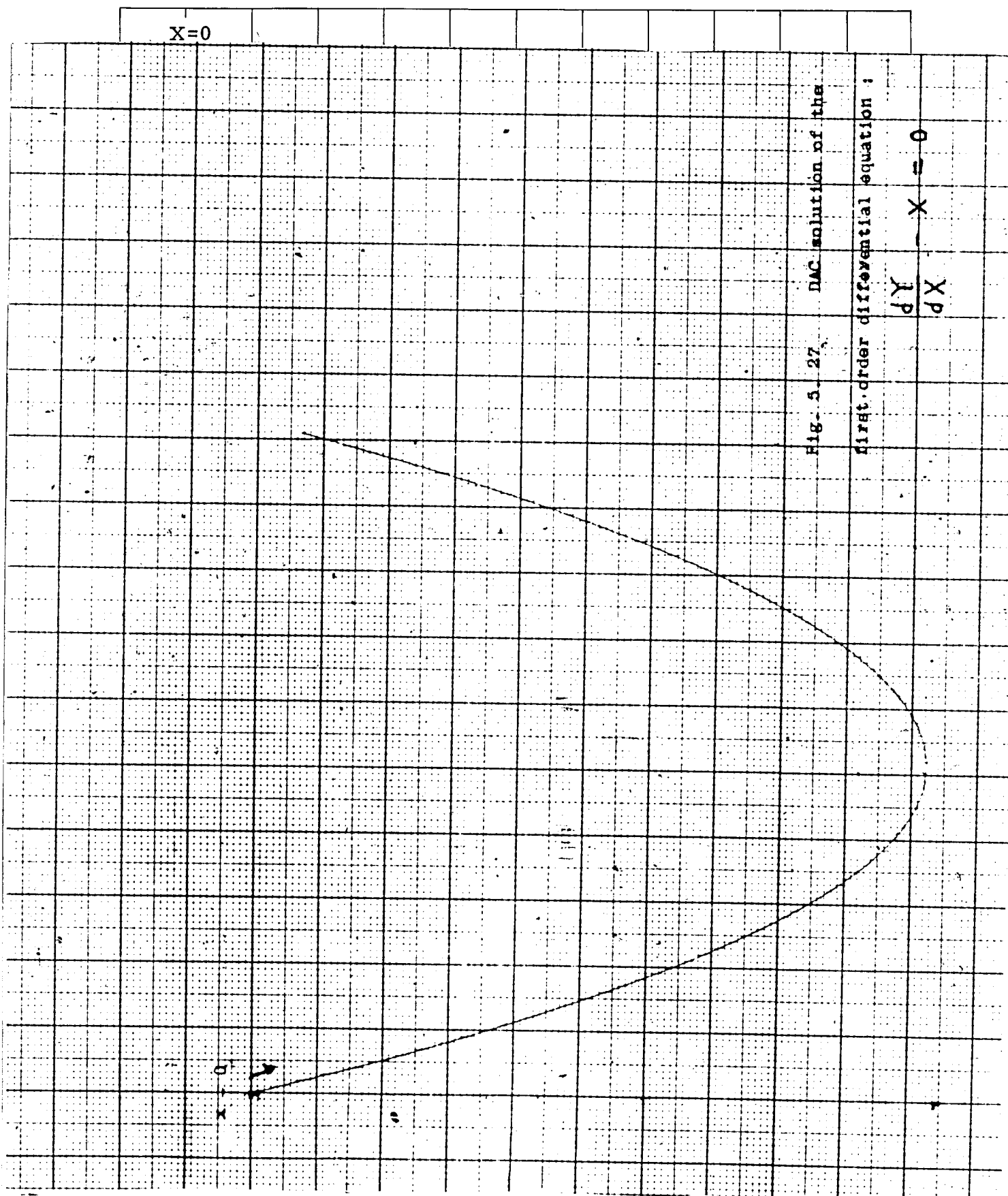


Fig. 5. 27 DAC solution of the first order differential equation:

$$\frac{dY}{dX} - X = 0$$

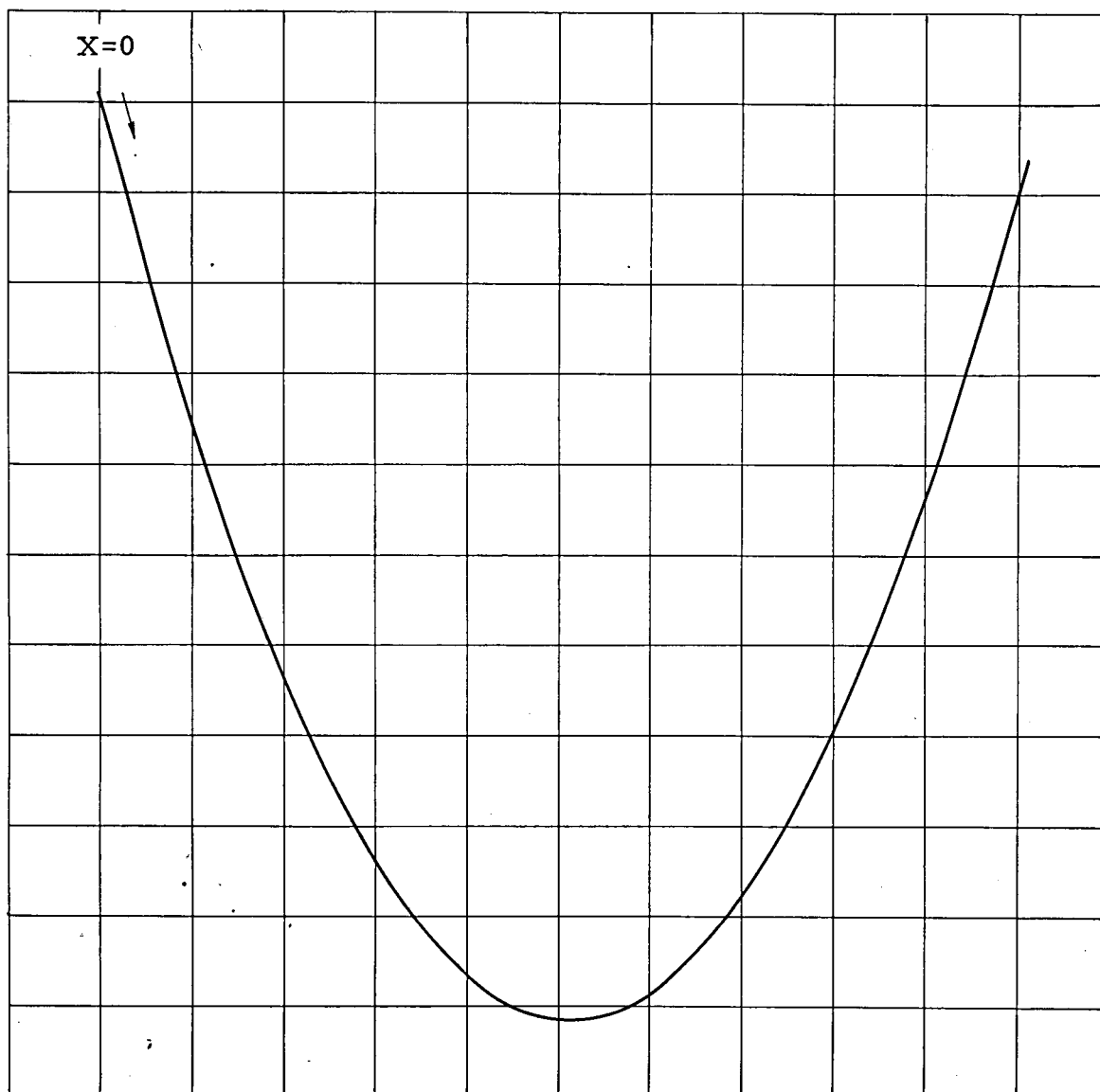


Table 5.10 Frequency of sine wave vs multiplication factor k.

k	f (k)	k	f (k)
0	0.003 c/s	10	3.068
1	0.006	11	6.136
2	0.012	12	12.272
3	0.024	13	24.544
4	0.048	14	49.088
5	0.096	15	98.176
6	0.192	16	196.352
7	0.384	17	392.704
8	0.768		
9	1.534		

As k increases the solution tends to diverge. This problem is discussed in later sections. Shown in Fig. 5.26 is a phase plane locus of the solution for k = 6, which is a complete circle.

The final example is the equation of a parabola

$$\frac{dz}{dx} - X = 0 \quad (5.45)$$

The result obtained by DAC - 1 is shown in Fig. 5.27

## 5.5 Accuracy and Computation speed of DAC

As the operation of DAC is based on the difference equation approximation of the differential equation, large step of integration which increases computation speed results less accuracy. When the step is made small to increase the accuracy the computation speed reduces. This relation between the accuracy and the computation speed will be examined in this section.

### 5.5.1 Maximum Rate of Change of Variables

As the magnitude of increment of DAC is fixed at  $2^{-18}$  the maximum rate of change of variable is  $2^{-18}$  per iteration time, or one in 52.43 seconds. When the effective length of the variable is shortened k bits the maximum rate of change of variable increases to  $2^{k-18}$  per iteration time.



### 5.5.2 Truncation Error 72)

The truncation error due to the difference approximation is a serious problem in DAC as this is strongly related to the computation speed.

The method of circle test used in analog computer technology is applied to this problem.

The second order differential equation which follows is solved by the computer circuit of Fig. 5.28.

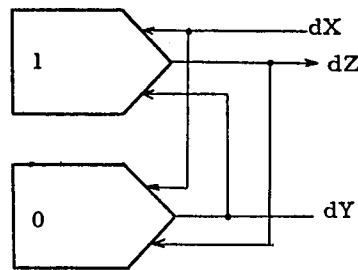


Fig. 5.28 DAC circuit for calculating eq. (5.46)

$$\left. \begin{aligned} \frac{dZ}{dX} &= Y \\ \frac{dY}{dX} &= -Z \end{aligned} \right\} \quad (5.46)$$

$$X = 0, Y = 1, Z = 0$$

This is written in Euler's approximation as

$$Z_{n+1} = Z_n + Y_n \cdot h \quad (5.47)$$

$$Y_{n+1} = Y_n - Z_n \cdot h \quad (5.48)$$

$$Y_0 = 1 \quad Z_0 = 0 \quad (5.49)$$

where  $h = 2^{k-18}$  (5.49)

The solutions of this difference equation are written

$$Y_n = C_1 \lambda^n \quad (5.50)$$

$$Z_n = C_2 \lambda^n$$

Substituting these into eq. (5.47) the following characteristic equation is obtained

$$\begin{vmatrix} 1-\lambda & h \\ -h & 1-\lambda \end{vmatrix} = 0 \quad (5.51)$$

The characteristic root obtained from this equation is

$$\lambda = 1 \pm jh \quad (5.52)$$

The solution of eq. (5.47) is then

$$\begin{aligned} Z_n &= \frac{1}{2j} \left\{ (1 + jh)^n - (1 - jh)^n \right\} \\ &= \mu^n \sin n\theta \end{aligned} \quad (5.53)$$

where

$$\mu = \sqrt{1 + h^2} \quad (5.54)$$

$$\theta = \tan^{-1} h \quad (5.55)$$

The solution of the difference equation of eq. (5.47) has errors both in amplitude and phase to the solution of the original differential equation eq. (5.46),  $\sin X$ . As  $\mu$  is larger than unity the amplitude of  $Z_n$  increases as  $n$  increases.

The phase error is represented by the relative phase error  $\epsilon_T$  and the amplitude error is represented by relative increase in amplitude per one cycle  $\epsilon_A$ . They are obtained in the percent case as follow.

$$\epsilon_T = \frac{n\theta - nh}{nh} = \frac{1}{h} \tan^{-1} h - 1 \quad (5.56)$$

$$\epsilon_A = \frac{\mu^{\frac{(m+\frac{3}{2})\pi}{\theta}} - \mu^{\frac{(m-\frac{1}{2})\pi}{\theta}}}{\mu^{\frac{(m-\frac{1}{2})\pi}{\theta}}} = \mu^{\frac{2\pi}{\theta}} - 1 \quad (5.57)$$

when  $h$  is small they are approximated by

$$\epsilon_T \cong -\frac{1}{3} h^2 \quad (5.58)$$

$$\epsilon_A \cong \pi h \quad (5.59)$$

$\epsilon_T$  and  $\epsilon_A$  for generating sinusoidal function of  $f$  (c/s) by Euler's approximation

formula are shown in Table 5.11.

Table 5.11

Phase error and amplitude error of Euler integration of eq. (5.46)

$f$ c/s	number of steps in one cycle	$h$	$\epsilon_T$	$\epsilon_A$	$N$	$\tau$
0.01	500,000	$4\pi \times 10^{-6}$	$-0.53 \times 10^{-10}$	$3.95 \times 10^{-5}$	2,320	64.5 hr.
0.1	50,000	$4\pi \times 10^{-5}$	$-0.53 \times 10^{-8}$	$3.95 \times 10^{-4}$	232	38.2 mm
1	5,000	$4\pi \times 10^{-4}$	$-0.53 \times 10^{-6}$	$3.95 \times 10^{-3}$	23.2	23.2 sec.
5	1,000	$2\pi \times 10^{-3}$	$-0.132 \times 10^{-4}$	$1.98 \times 10^{-2}$	4.64	9.28 "
10	500	$4\pi \times 10^{-3}$	$-0.53 \times 10^{-4}$	$3.95 \times 10^{-2}$	2.32	0.232"

The number of cycles  $N$  and the time elapsed  $\tau$  before the amplitude diverges by 10 % are also shown.

As actually DAC uses the trapezoidal integration formula, the machine equation for the differential equation  $\frac{e_n}{e_{gv}}$  (5.46) is

$$\begin{aligned} Z_{n+1} &= Z_n + Y_n \cdot h + \frac{1}{2} (Y_n - Y_{n-1}) h \\ Y_{n+1} &= Y_n - Z_n \cdot h - \frac{1}{2} (Z_n - Z_{n-1}) h \end{aligned} \quad (5.60)$$

The characteristic equation of this difference equation is

$$\begin{vmatrix} 1 - \lambda & (1 + \frac{\lambda-1}{2\lambda}) h \\ -(1 + \frac{\lambda-1}{2\lambda}) h & 1 - \lambda \end{vmatrix} = 0 \quad (5.61)$$

The characteristic roots of the above equation are

$$\lambda_1 = 1/2 \left\{ 1 + 3/2 jh + \sqrt{1 + jh - 9/4 h^2} \right\} \quad (5.62)$$

$$\lambda_2 = 1/2 \left\{ 1 + 3/2 jh - \sqrt{1 + jh - 9/4 h^2} \right\} \quad (5.63)$$

$$\lambda_3 = 1/2 \left\{ 1 - 3/2 jh + \sqrt{1 - jh - 9/4 h^2} \right\} \quad (5.64)$$

$$\lambda_4 = 1/2 \left\{ 1 - 3/2 jh - \sqrt{1 - jh - 9/4 h^2} \right\} \quad (5.65)$$

Neglecting smaller quantities than  $h^2$  they are obtained as

$$\lambda_1 = 1 - 1/2 h^2 + jh \quad (5.66)$$

$$\lambda_2 = 1/2 h^2 + 1/2 jh \quad (5.67)$$

$$\lambda_3 = 1 - 1/2 h^2 - jh \quad (5.68)$$

$$\lambda_4 = 1/2 h^2 - 1/2 jh \quad (5.69)$$

As  $\lambda_2$  and  $\lambda_4$  are much smaller than  $\lambda_1$  and  $\lambda_3$  the solutions belonging to these two roots vanish in a few steps of integration. The remaining two roots  $\lambda_1$  and  $\lambda_3$  affect the accuracy of the solution. The solution of eq. (5.60) is therefore written in a similar form to eq. (5.53). It is

$$Z^n = \mu'^n \sin n \theta' \quad (5.70)$$

$$\mu' = \sqrt{1 + \frac{1}{4} h^4} \quad (5.71)$$

$$\theta' = \tan^{-1} \frac{h}{1 - \frac{1}{2} h^2} \quad (5.72)$$

The phase error and the amplitude error are obtained as

$$\epsilon_{\tau'} = \frac{1}{h} \tan^{-1} \frac{h}{1 - \frac{1}{2} h^2} - 1 \cong \frac{1}{6} h^2 \quad (5.73)$$

$$\epsilon_{A'} = \mu^{\frac{2\pi}{\theta'}} - 1 \cong \frac{3}{4} h^3 \quad (5.74)$$

These errors are calculated for various frequencies of the sinusoidal function to be generated by DAC and are shown in Table 5.12

Table 5.12

Phase error and amplitude error of trapezoidal integration of eq. (5.46)

$f_c/s$	number of steps in one cycle	$h$	$\epsilon_{\tau}$	$\epsilon_A$	$N$	$\tau$
1	5,000	$4\pi \times 10^{-4}$	$0.27 \times 10^{-6}$	$1.57 \times 10^{-9}$	6,370,000	1,769 hr.
10	500	$4\pi \times 10^{-3}$	$0.27 \times 10^{-4}$	1.57	6,370	10.6 mm
50	100	$2\pi \times 10^{-2}$	$0.66 \times 10^{-3}$	1.96	510	10.2 sec
100	50	$4\pi \times 10^{-2}$	$0.27 \times 10^{-2}$	1.57	6.37	0.0637 sec.

In this table we see that the sinusoidal wave of 50 c/s is generated almost stably by DAC. This fact states that DAC is superior to dc analog computers also in computation speed.

The above discussions are summarized as follows. When an ordinary differential equation of  $n$ th order

$$a_0 \frac{d^n y}{dx^n} + a_1 \frac{d^{n-1} y}{dx^{n-1}} + \dots + a_{n-1} \frac{dy}{dx} + a_n y = 0 \quad (5.75)$$

is solved by Euler's integration formula the characteristic equation of the difference equation is

$$\lambda_0 s^n + \lambda_1 s^{n-1} + \dots + \lambda_{n-1} s + \lambda_n = 0 \quad (5.76)$$

where

$$s = \frac{\lambda - 1}{h} \quad (5.77)$$

Let the characteristic roots of the original differential equation be  $\lambda_k$ , where  $k = 1, 2, \dots, n$  then the characteristic roots of the difference equation are obtained as

$$\lambda_K = 1 + S_K \cdot h \quad (5.78)$$

If we use the expressions

$$S_K = \alpha_K + j\beta_K \quad (5.79)$$

$$\lambda_K = \mu_K e^{j\theta_K} \quad (5.80)$$

we obtain

$$\mu_K = \sqrt{1 + 2\alpha_K h + (\alpha_K^2 + \beta_K^2)h^2} \quad (5.81)$$

$$\theta_K = \tan^{-1} \frac{\beta_K h}{1 + \alpha_K h} \quad (5.82)$$

If we define the relative amplitude error  $\varepsilon_A$  and the relative phase error  $\varepsilon_T$  for the transient term of the difference equation concerning a particular characteristic root  $k$  in a similar way done for the circle test, they are calculated as

$$\varepsilon_A = \frac{\mu^n - e^{\alpha_K n h}}{e^{\alpha_K n h}} \cong \frac{n}{2} (\beta_K^2 - \alpha_K^2) \cdot h^2 \quad (5.83)$$

$$\varepsilon_T = \frac{n\theta_K - \beta_K n h}{\beta_K n h} \cong \alpha_K h + (\alpha_K^2 - \frac{1}{3}\beta_K^2)h^2 \quad (5.84)$$

Similar calculation is performed for the amplitude error and the phase error of trapezoidal integration of eq. (5.75). For trapezoidal formula following equation is used instead of eq. (5.77)

$$S = \frac{\lambda - 1}{\left\{1 + \frac{1}{2}\left(1 - \frac{1}{\lambda}\right)\right\}h} \quad (5.85)$$

The characteristic roots of the difference equation corresponding to those of the original differential equation  $\lambda_K$  are calculated by neglecting smaller quantities than  $h^2$  as follow.

$$\lambda_{K1} \cong 1 + S_K h + \frac{1}{2} S_K^2 h^2 \quad (5.86)$$

$$\lambda_{K2} \cong \frac{1}{2} S_K h - \frac{1}{2} S_K^2 h^2 \quad (5.87)$$

As the second root is very small and the transient term due to this root vanishes rapidly only the first root is considered in the following discussion.

Using the expression eq. (5.79) and eq. (5.80) results

$$\mu_K = \sqrt{1 + 2\alpha_K h + 2\alpha_K^2 h^2 + \alpha_K(\alpha_K^2 + \beta_K^2)h^3 + \frac{1}{4}(\alpha_K^2 + \beta_K^2)^2 h^4} \quad (5.88)$$

$$\theta_K = \tan^{-1} \frac{\beta_K(1 + \alpha_K h)h}{1 + \alpha_K h + \frac{1}{2}(\alpha_K^2 - \beta_K^2)h^2} \quad (5.89)$$

Finally the amplitude error  $\varepsilon_A'$  and the phase error  $\varepsilon_T'$  are obtained in

the following approximated formula

$$\varepsilon_A' \cong \left\{ \frac{1}{2} \alpha_K (\beta_K^2 - \frac{1}{3} \alpha_K^2) h^3 + \frac{1}{8} (\alpha_K^4 - 6 \alpha_K^2 \beta_K^2 + \beta_K^4) h^4 \right\} n \quad (5.89)$$

$$\varepsilon_T' \cong -\frac{1}{2} (\alpha_K^2 - \frac{1}{3} \beta_K^2) h^2 \quad (5.90)$$

Before concluding the discussion let us consider additional characteristic root introduced by the coefficient multiplier. The operation of a coefficient multiplier is represented by the next difference equation.

$$Y_{n+1} = Y_n + k (Z_n - Z_{n-1}) \quad (5.91)$$

Consider the computer circuit of DAC shown in Fig. 5.29 which solves following differential equation.

$$\frac{d^2 U}{dX^2} + k U = 0 \quad (5.92)$$

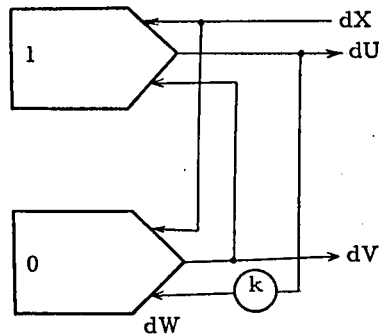


Fig. 5.29 DAC circuit for calculating eq. (5.92)

The difference equations of the computer circuit which uses Euler's integrators are

$$U_{n+1} = U_n + V_n h \quad (5.93)$$

$$V_{n+1} = V_n - W_n h \quad (5.94)$$

$$W_{n+1} = W_n + k (U_n - U_{n-1}) \quad (5.95)$$

The characteristic equation of this set of difference equations is as follows.

$$\begin{vmatrix} 1-\lambda & h & 0 \\ 0 & 1-\lambda & -h \\ K(1-\frac{1}{\lambda}) & 0 & 1-\lambda \end{vmatrix} = 0 \quad (5.96)$$

Four characteristic roots are obtained from this equation. Since  $kh^2$  is small they are approximately given as follow.

$$\lambda_1 \cong 1 + \frac{1}{2}Kh^2 + j\sqrt{K} \cdot h \quad (5.97)$$

$$\lambda_2 \cong 1 + \frac{1}{2}Kh^2 - j\sqrt{K} \cdot h \quad (5.98)$$

$$\lambda_3 \cong -Kh^2 \quad (5.99)$$

$$\lambda_4 = 1 \quad (5.100)$$

The third characteristic root is small enough to be neglected and the fourth one gives a constant term. Therefore the first two characteristic roots are the significant ones. The solution of the difference equation is written as before in the following form

$$U = \mu^n \sin n\theta \quad (5.101)$$

where

$$\mu = \sqrt{1 + 2Kh^2 + \frac{1}{4}K^2h^4} \quad (5.102)$$

$$\theta = \tan^{-1} \frac{\sqrt{K} \cdot h}{1 + \frac{1}{2}Kh^2} \quad (5.103)$$

The amplitude error and the phase error are

$$\varepsilon_A = \mu^{\frac{2\pi}{\sqrt{K} \cdot h}} - 1 \cong 2\pi\sqrt{K} \cdot h \quad (5.104)$$

$$\varepsilon_T = \frac{n\theta - n\sqrt{K} \cdot h}{n\sqrt{K} \cdot h} \cong -\frac{5}{6}Kh^2 \quad (5.105)$$

The time lag caused by the coefficient multiplier increases the errors by a factor of two.

### 5.5.3 Round-Off Error

Another significant error of the computation of DAC is the round-off error due to a finite length of the registers and the fixed <sup>quantity</sup> ~~quantity~~ of the incremental output signals of the computing elements. The round-off error becomes a serious problem especially when the effective length of the Y register is shorter than eighteen bits.

Typical effect of the round-off error appears when the solution by DAC asymptotes a finite value. For example when the following differential equation

$$\left. \begin{aligned} \frac{dZ}{dX} + Z &= 0 \\ X = 0, \quad Z &= Z_0 \end{aligned} \right\} \quad (5.106)$$

is solved on DAC the halving time of the solution considerably decreases as it approaches zero while that the rigorous solution is a constant. Consider the integrater solving eq. (5.106) shown in Fig. 5.30.

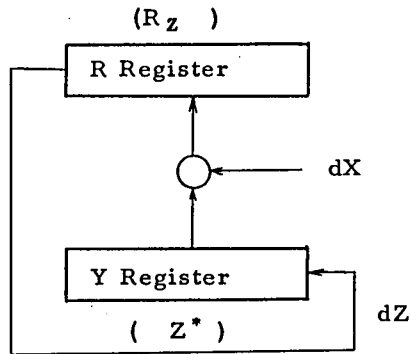


Fig. 5.30 Block diagram of an integrater solving eq. (5.106)

As  $dX$  signal is applied at each iteration time content of  $Y$  register is added into the  $R$  register and the output from the  $R$  register subtracts the content of  $Y$  register. Let the iteration time be  $\tau_0$  the time necessary to subtract the last bit of the  $Y$  register  $\tau_1$  is obtained as

$$\tau_1 = 2^{18} \tau_0 \quad (5.107)$$

because  $2^{18}$  times of addition of  $2^{-18}$  stored in  $Y$  register to register make an output from  $R$  register. Likewise the halving time of the second least significant bit of  $Y$  register  $\tau_2$  is calculated

$$\tau_2 = \frac{1}{2} \tau_1 \quad (5.108)$$

because when  $2^{-17}$  is stored in  $Y$  register  $2^{17}$  times of addition of this quantity to  $R$  register make an output from  $R$  register which changes the content of  $Y$  register  $2^{-18}$ . The halving time of the third least significant bit of  $Y$  register is calculated in a following way. Initially  $2^{-16}$  exists in  $Y$  register.  $2^{16}$  times of addition of this quantity into  $R$  register result an output from  $R$  register and the content of  $Y$  register becomes  $(2^{-17} + 2^{-18})$ .

Another  $\tau_1/3$  seconds are necessary to change the halving time of this case; that is

$$\tau_3 = \left( \frac{1}{3} + \frac{1}{4} \right) \tau_1 \quad (5.109)$$

In a similar way the halving times for the more significant bits are obtained as follow.



$$\tilde{\tau}_4 = \left( \frac{1}{5} + \frac{1}{6} + \frac{1}{7} + \frac{1}{8} \right) \tilde{\tau}_1 \quad (5.110)$$

$$\tilde{\tau}_5 = \left( \frac{1}{9} + \frac{1}{10} + \frac{1}{11} + \frac{1}{12} + \frac{1}{13} + \frac{1}{14} + \frac{1}{15} + \frac{1}{16} \right) \tilde{\tau}_1 \quad (5.111)$$

$$\tilde{\tau}_n = \tilde{\tau}_1 \cdot \sum_{i=1}^{2^{n-2}} \frac{1}{2^{n-2}+i} \quad (5.112)$$

These values are shown in Fig. 5.31

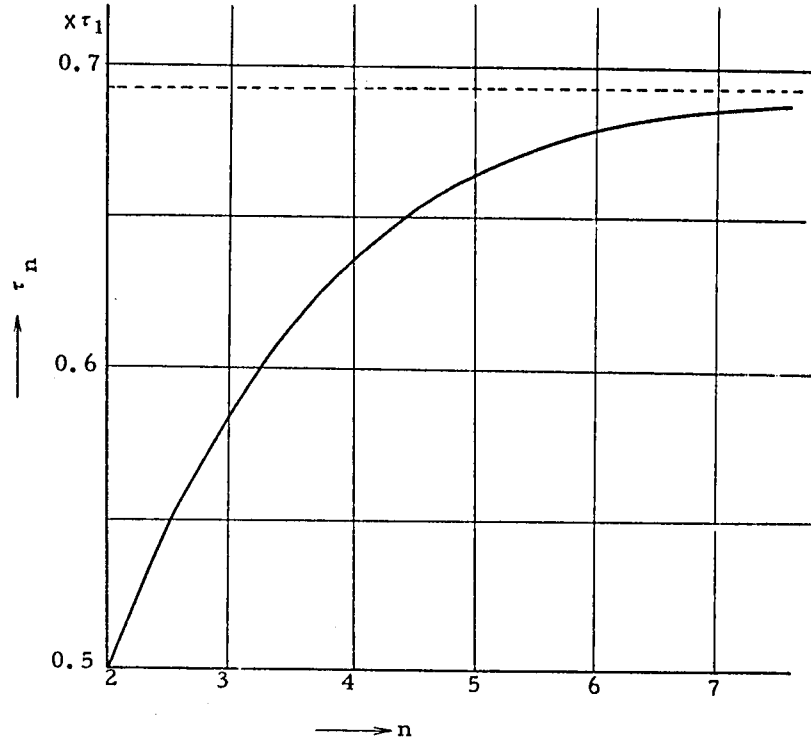


Fig. 5.31 Halving times for different numbers of bits in Y register.

As  $n$  increases these values approach  $\tilde{\tau}_1 \log_e 2$  which is the halving time of the rigorous solution.

The effect of the round-off error in the computation of DAC is now discussed in more general case. The differential equation

$$\frac{dZ}{dX} = Y \quad (5.113)$$

is approximated by the following difference equation by Euler's formula.

$$Z_{n+1} - Z_n = Y_n h \quad (5.114)$$

the error of which is only a truncation error. Now consider that an integrater is connected to another integrater as shown in Fig. 5.32

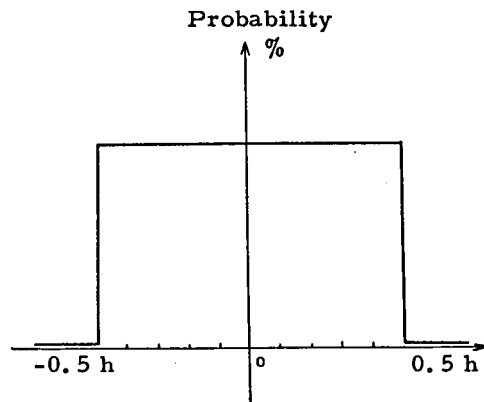


Fig. 5.32 Probability density of the round-off error.

As R register of the first integrater stores the remainder of the quantity stored in Y register of the second integrater the operation of the second integrater has an error caused by not adding this remainder to its own R register. This is the round-off error. By considering this round-off error the variables are written in the following way.

$$Y_n = Y_n^* + R_{Yn} \quad (5.115)$$

$$Z_n = Z_n^* + R_{Zn} \quad (5.116)$$

where  $Y_n$  and  $Z_n$  are numbers stored in Y registers, and  $R_{Yn}$  and  $R_{Zn}$  are those in R registers.

Obviously  $R_n = O(h) \quad (5.117)$

Using these relations the operation of the integrater is described by the following equation.

$$\begin{aligned} Z_{n+1} - Z_n &= Y_n^* h \\ &= Y_n h - R_{Yn} h \end{aligned} \quad (5.118)$$

As a particular example let us consider the effect of the round-off error when

$$Y = -Z \quad (5.119)$$

eq. (5.118) then becomes

$$Z_{n+1} = (1-h) Z_n - R_n h \quad (5.120)$$

Considering  $Z_n$  and  $R_n$  staircase functions of time the Laplace transform of this difference equation is written

$$\{1 - (1-h) z^{-1}\} Z(s) = -z^{-1} R(s) h \quad (5.121)$$

which is solved as

$$Z(s) = \frac{-z^{-1} R(s) h}{1 + (1-h) z^{-1}} \quad (5.122)$$

where

$$z^{-1} = e^{-s\tau_0} \quad (5.123)$$

substituting

$$R(s) = \sum z^{-n} R_n \quad (5.124)$$

and

$$Z(s) = \sum z^{-n} Z_n \quad (5.125)$$

into eq. (5.122), we obtain

$$Z_n = h \{ (1-h)^{n-1} R_0 + (1-h)^{n-2} R_1 + (1-h)^{n-3} R_2 + \dots + (1-h) R_{n-2} + R_{n-1} \} \quad (5.126)$$

As  $R_n$  is a random number with the standard deviation  $\sigma_0$ , the standard deviation of  $Z_n$  is calculated as

$$\begin{aligned} \sigma(n) &= h \sqrt{1 + (1-h)^2 + (1-h)^4 + \dots + (1-h)^{2n-2}} \\ &= h \sqrt{\frac{1 - (1-h)^{2n}}{2h - h^2}} \cdot \sigma_0 \end{aligned} \quad (5.127)$$

When  $n$  is infinite  $\sigma(n)$  becomes  $\sigma_z$

$$\sigma_z = \sqrt{\frac{h}{2}} \cdot \sigma_0 \quad (5.128)$$

In the foregoing discussion the round-off error is considered to be

random. Actually round off error is by no means random but has a definite form of time function. Generally the round-off error is the difference of the continuous function and the quantized staircase function. Although consideration of round-off error as a random number is allowable in the macroscopic discussion of the error, consideration of the detailed waveform will be required for explicit calculation of the error.

In eq. (5.128)  $\sigma_o$  denotes the standard deviation of  $R_n$ . This is calculated as follows.

The distribution of round-off-error is as shown in Fig. 5.32.

Therefore

$$\sigma_o = \sqrt{\frac{1}{h} \int_{-\frac{h}{2}}^{\frac{h}{2}} x^2 dx} = 0.29h \quad (5.129)$$

An example of calculation is shown in Fig. 5.33, where

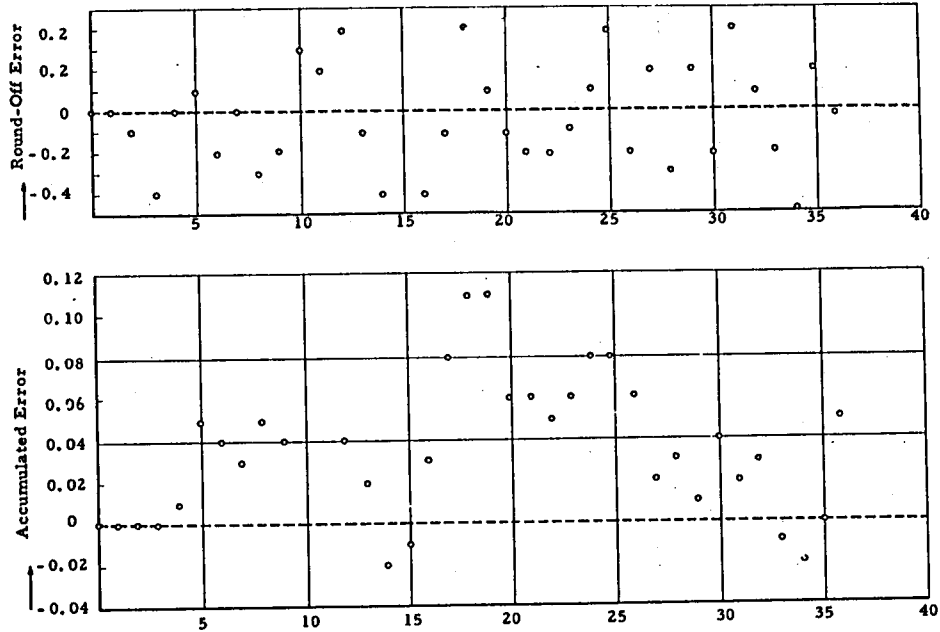


Fig. 5.33 Round-off error and the accumulated error in solving eq. (5.120)

$$Z_0 = 100 \quad \text{and} \quad h = 0.1$$

Now the round-off error of a general linear differential equation is investigated. The general linear differential equation is written as

$$\frac{d}{dX} \begin{pmatrix} Y_1 \\ Y_2 \\ \vdots \\ Y_N \end{pmatrix} = (a_{ij}) \cdot \begin{pmatrix} Y_1 \\ Y_2 \\ \vdots \\ Y_N \end{pmatrix} - \begin{pmatrix} F_1 \\ F_2 \\ \vdots \\ F_N \end{pmatrix} \quad (5.130)$$

or in vectorial form

$$\frac{d\vec{Y}}{dX} = A \cdot \vec{Y} - \vec{F} \quad (5.131)$$

The difference equation by Euler's formula considering round-off error is

$$\vec{Y}_{n+1} = \vec{Y}_n + h (A \cdot \vec{Y}_n - A \cdot \vec{R}_n - \vec{F}_n) \quad (5.132)$$

Neglecting  $\vec{F}_n$  to consider only error term and taking Laplace transform this equation reduces to the following form.

$$[E - Z^{-1}(E + hA)] \cdot \vec{Y}(s) = -Z^{-1} h A \cdot \vec{R}(s) \quad (5.133)$$

where

$$\vec{Y}(s) = \sum Z^{-n} \vec{Y}_n, \quad \vec{R}(s) = \sum Z^{-n} \vec{R}_n \quad (5.134)$$

Solving this equation for  $\vec{Y}(s)$ , we obtain

$$\begin{aligned} \vec{Y}(s) &= -Z^{-1} h [E - Z^{-1}(E + hA)]^{-1} \cdot A \cdot \vec{R}(s) \\ &= -Z^{-1} h [E + Z^{-1}(E + hA) + Z^{-2}(E + hA)^2 + \dots \\ &\quad + Z^{-n}(E + hA)^n + \dots] \cdot A \cdot \vec{R}(s) \\ &= -h \sum Z^{-n} [E \cdot \vec{R}_{n-1} + (E + hA) A \cdot \vec{R}_{n-2} + \dots + (E + hA)^{n-1} A \cdot \vec{R}_0] \end{aligned} \quad (5.135)$$

Therefore we obtain

$$\vec{Y}_n = -h [A \cdot \vec{R}_{n-1} + (E + hA) A \cdot \vec{R}_{n-2} + \dots + (E + hA)^{n-1} A \cdot \vec{R}_0] \quad (5.136)$$

Denoting

$$(E + hA)^k A = \begin{pmatrix} K_{11} & K_{12} & \dots & K_{1N} \\ K_{21} & K_{22} & \dots & K_{2N} \\ \vdots & \vdots & \ddots & \vdots \\ K_{N1} & K_{N2} & \dots & K_{NN} \end{pmatrix} \quad (5.137)$$

An element of  $\vec{Y}_n$  of eq. (5.136) is written as

$$Y_{in} = -h(o_{i1} o_{i2} \dots o_{iN}) \cdot \begin{pmatrix} R_{1n-1} \\ R_{2n-1} \\ \vdots \\ R_{Nn-1} \end{pmatrix} - h(l_{i1} l_{i2} \dots l_{iN}) \cdot \begin{pmatrix} R_{1n-2} \\ R_{2n-2} \\ \vdots \\ R_{Nn-2} \end{pmatrix} \\ \dots \dots \dots - h((n-1)_{i1} \dots (n-1)_{iN}) \cdot \begin{pmatrix} R_{10} \\ R_{20} \\ \vdots \\ R_{N0} \end{pmatrix} \quad (5.138)$$

When  $R_{10}, R_{20}, \dots, R_{N, n-1}$  are considered random numbers of the standard deviation of  $\mathcal{A}_0$  the standard deviation of  $Y_{in}$  is calculated as

$$\mathcal{A}_i \quad \text{in the following equation} \\ \mathcal{A}_i = h \mathcal{A}_0 \sqrt{0_{i1}^2 + 0_{i2}^2 + \dots + 0_{iN}^2 + \dots + K_{i1}^2 + K_{i2}^2 + \dots + K_{iN}^2 + \dots + (n-1)_{iN}^2} \quad (5.139)$$

As  $K_{i1}^2 + K_{i2}^2 + \dots + K_{iN}^2$  is the  $i$  th diagonal element of the matrix

$$(E + hA)^K \cdot A \cdot A^t \cdot [(E + hA)^K]^t \quad (5.140)$$

$\mathcal{A}_i$  is finally obtained as

$$\mathcal{A}_i = h \mathcal{A}_0 \sqrt{S_i} \quad (5.141)$$

Where  $S_i$  is the  $i$  th diagonal element of the matrix

$$A \cdot A^t + (E + hA) \cdot A \cdot A^t (E + hA)^t + \dots + (E + hA)^{n-1} \cdot A \cdot A^t [(E + hA)^{n-1}]^t \quad (5.142)$$

As an example of application of eq. (5.141) the effect of the round-off error of the second order differential equation is estimated.

$$\left. \begin{aligned} \frac{dY}{dX} &= Z \\ \frac{dZ}{dX} &= -Y \end{aligned} \right\} \quad (5.143)$$

For this equation

$$A = \begin{pmatrix} 0 & 1 \\ -1 & 0 \end{pmatrix} \quad (5.144)$$

$$E + hA = \begin{pmatrix} 1 & h \\ -h & 1 \end{pmatrix} \quad (5.145)$$

$$\text{Therefore} \quad A \cdot A^t = E \quad (5.146)$$

$$(E + hA) (E + hA)^t = (1 + h^2) \cdot E \quad (5.147)$$

and the diagonal element of eq. (5.140) is readily obtainable as  $(1 + h^2)^k$ ,

Therefore

$$\begin{aligned} S_1 = S_2 &= 1 + (1+h^2) + (1+h^2)^2 + \dots + (1+h^2)^{n-1} \\ &= \frac{(1+h^2)^n - 1}{h^2} \end{aligned} \quad (5.148)$$

Finally the standard deviations of Y and Z are obtained from eq. (5.141) as

$$\sigma_1(n) = \sigma_2(n) = \sigma_0 \sqrt{(1+h^2)^n - 1} \quad (5.149)$$

In contrast to the previous example of the first order differential equation the standard deviation diverges as steps of integration proceed. In Fig. 5.34

$\sigma_1(n)$  is plotted against n.

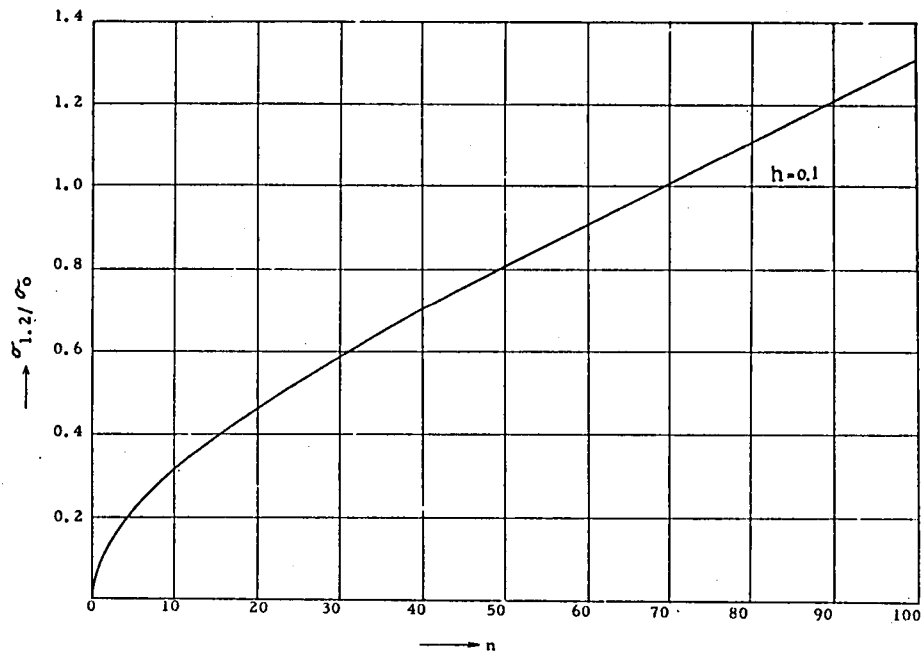


Fig. 5.34 Standard deviation of the accumulated error caused by rounding-off error of the Euler integration of eq. (5.143).

The round-off error of the trapezoidal integrator is more complex and will not be discussed in this thesis. Only the effect of the round-off error written in Z transform is shown below.

$$\vec{Y}(s) = hZ^{-1} \left( \frac{3}{2} - \frac{1}{2}Z^{-1} \right) [E - Z \{ E + h(\frac{3}{2} - \frac{1}{2}Z)A \}]^{-1} A \cdot \vec{R} \quad (5.150)$$

## 5.6 Incremental Calculus 73)

The DAC is an incremental computer which executes any computation by incremental calculus. As will be seen in the following examples almost any differentiable function can be generated by incremental calculus.

### 5.6.1 Polynomial

$$f(x) = a_0 + a_1x + a_2x^2 + \dots + a_nx^n \quad (5.151)$$

By successive differentiation we obtain following equations.

$$\left. \begin{aligned} f(0) &= a_0, & df &= f' dx \\ f'(0) &= a_1, & df' &= f'' dx \\ &----- &----- \\ f^{(n-1)}(0) &= (n-1)! a_{n-1}, & df^{(n-1)} &= f^{(n)}(x) dx \\ f^{(n)}(x) &= n! a_n \end{aligned} \right\} \quad (5.152)$$

By using these relations the computer circuit for generating eq. (5.15) is obtained as shown in Fig. 5.35.

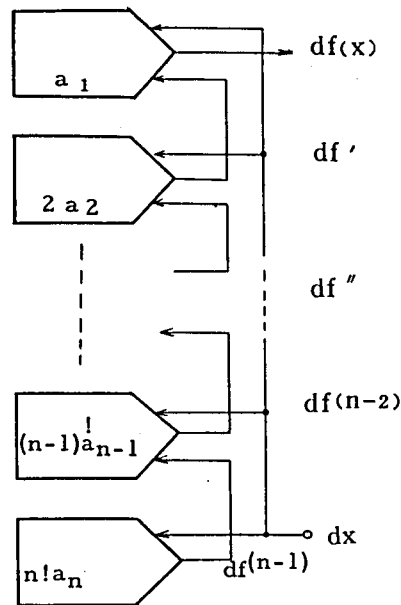


Fig. 5.35

DAC circuit for calculating eq. (5.151)

### 5.6.2 Rational Function

$$f(x) = \frac{a_0 + a_1 x + \dots + a_m x^m}{b_0 + b_1 x + \dots + b_n x^n} = \frac{M(x)}{N(x)} \quad (5.153)$$

By differentiating, we obtain

$$\left. \begin{aligned} df &= \frac{1}{N} dM - M d\left(\frac{1}{N}\right) \\ d\left(\frac{1}{N}\right) &= -\frac{1}{N^2} dN \\ d\left(\frac{1}{N^2}\right) &= -\frac{2}{N} d\left(\frac{1}{N}\right) \end{aligned} \right\} \quad (5.154)$$

As  $M(x)$  and  $N(x)$  are obtainable by the circuit of Fig. 5.35  $f(x)$  is calculated by the circuit of Fig. 5.36.



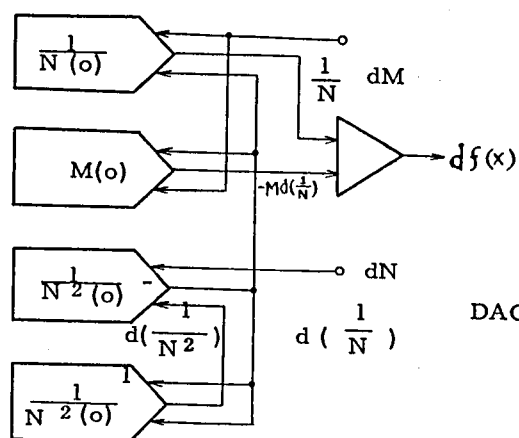


Fig. 5.36

DAC circuit for calculating eq. (5.153)

### 5.6.3 Coordinate Transformation

The coordinate transformation which is frequently necessitated in the fire control system and the tracking devices is one of the favorite tasks performed by the incremental calculus.

- (i) Transformation from Two-Dimensional Polar coordinate to Rectangular Coordinate.

$$\left. \begin{aligned} x &= r \cos \theta \\ y &= r \sin \theta \end{aligned} \right\} \quad (5.155)$$

By differentiation we obtain

$$\left. \begin{aligned} dx &= dr \cos \theta - y d\theta \\ dy &= dr \sin \theta + x d\theta \\ d(\cos \theta) &= -\sin \theta \cdot d\theta \\ d(\sin \theta) &= \cos \theta \cdot d\theta \end{aligned} \right\} \quad (5.156)$$

These relations are representable by the circuit of Fig. 5.37

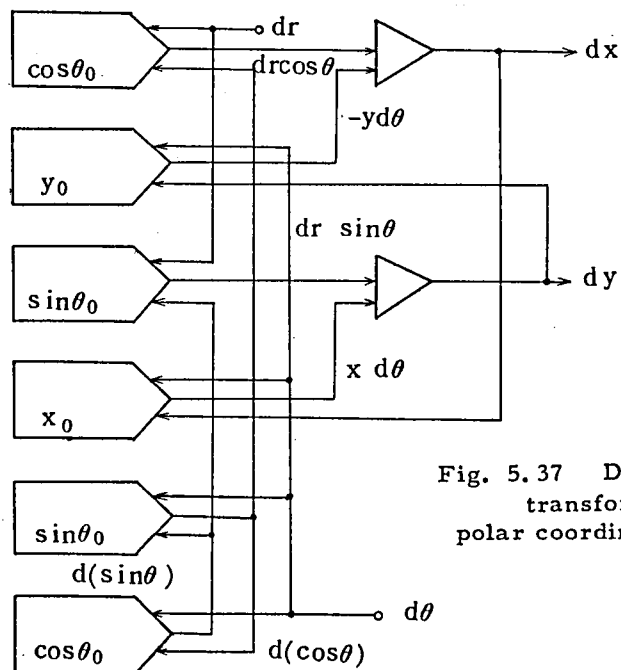


Fig. 5.37 DAC circuit for coordinate transformation from two-dimensional polar coordinate to rectangular coordinate.

(ii) Transformation from Two-Dimensional Rectangular Coordinate to Polar Coordinate

$$\begin{aligned} r &= \sqrt{x^2 + y^2} \\ \theta &= \tan^{-1} \frac{y}{x} \end{aligned} \quad (5.157)$$

By successive differentiation we obtain

$$\left. \begin{aligned} dr &= dx \cos \theta + dy \sin \theta \\ d\theta &= \frac{\cos \theta}{r} dy - \frac{\sin \theta}{r} dx \\ d\left(\frac{\cos \theta}{r}\right) &= -d\theta \left(\frac{\sin \theta}{r}\right) + d\left(\frac{1}{r}\right) \cos \theta \\ d\left(\frac{\sin \theta}{r}\right) &= d\theta \left(\frac{\cos \theta}{r}\right) + d\left(\frac{1}{r}\right) \sin \theta \\ d\left(\frac{1}{r}\right) &= -\left(\frac{1}{r}\right)^2 dr \\ d\left\{\left(\frac{1}{r}\right)^2\right\} &= \frac{2}{r} d\left(\frac{1}{r}\right) \end{aligned} \right\} \quad (5.158)$$

These relations are representable by ten integraters and four adders.

(iii) Transformation from Three-Dimensional Polar Coordinate to Rectangular Coordinate.

$$\left. \begin{aligned} x &= r \sin \theta \cos \phi \\ y &= r \sin \theta \sin \phi \\ z &= r \cos \theta \end{aligned} \right\} \quad (5.159)$$

Successive differentiation leads to the following set of equations.

$$\left. \begin{aligned} dx &= dr \sin \theta \cos \phi + d\theta z \cos \phi - d\phi y \\ dy &= dr \sin \theta \sin \phi + d\theta z \sin \phi + d\phi x \\ dz &= dr \cos \theta - d\theta \cdot r \sin \theta \\ d(\sin \theta \cos \phi) &= d\theta \cos \theta \cdot \cos \phi - d\phi \sin \theta \cdot \sin \phi \\ d(\sin \theta \sin \phi) &= d\theta \cos \theta \cdot \sin \phi + d\phi \sin \theta \cdot \cos \phi \\ d(\cos \theta \cos \phi) &= -d\theta \sin \theta \cdot \cos \phi - d\phi \cos \theta \cdot \sin \phi \\ d(\cos \theta \sin \phi) &= -d\theta \sin \theta \cdot \sin \phi + d\phi \cos \theta \cdot \cos \phi \\ d(z \cos \phi) &= dz \cos \phi - d\phi z \sin \phi \\ d(z \sin \phi) &= dz \sin \phi + d\phi z \cos \phi \\ d(\cos \phi) &= -d\phi \sin \phi \end{aligned} \right\} \quad (5.160)$$

$$d(\sin \phi) = d\phi \cos \phi$$

$$d(r \sin \theta) = dr \sin \theta + d\theta \cdot r$$

$$d(\cos \theta) = -d\theta \sin \theta$$

$$d(\sin \theta) = d\theta \cos \theta$$

By twenty-six integraters and ten adders above relations are representable.

(iv) Tracking Problem in Two-Dimensional Space

Rectangular coordinate (x, y) is to be calculated from  $r_1$  and  $r_2$  in Fig. 5.38.

$$\left. \begin{aligned} r_1 &= \sqrt{(x-L)^2 + y^2} \\ r_2 &= \sqrt{(x+L)^2 + y^2} \end{aligned} \right\} \quad (5.161)$$

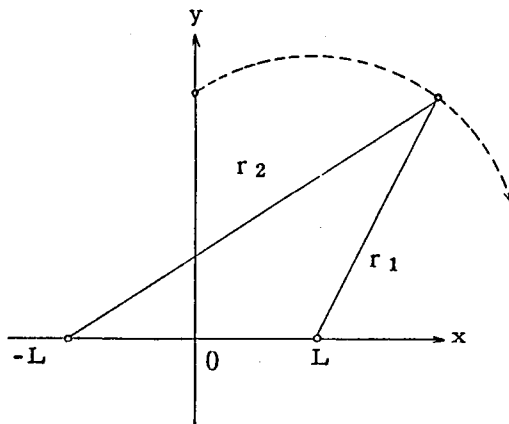


Fig. 5.38 Tracking problem in two dimensional space.

Rewriting these equations leads to

$$\left. \begin{aligned} X &= \frac{1}{4L} (r_2^2 - r_1^2) \\ Y^2 &= \frac{1}{2} (r_1^2 + r_2^2) - X^2 - L^2 \end{aligned} \right\} \quad (5.162)$$

By successive differentiation the following equations result.

$$\begin{aligned}
 dx &= \frac{1}{2L} (r_2 dr_2 - r_1 dr_1) \\
 d(y^2) &= r_1 dr_1 + r_2 dr_2 - 2x dx \\
 dy &= \frac{1}{2y} d(y^2) \\
 d\left(\frac{1}{y}\right) &= -\left(\frac{1}{y}\right)^2 dy \\
 d\left\{\left(\frac{1}{y}\right)^2\right\} &= \frac{2}{y} d\left(\frac{1}{y}\right)
 \end{aligned}
 \tag{5.163}$$

These relations are representable by the computer circuit of Fig. 5.39.

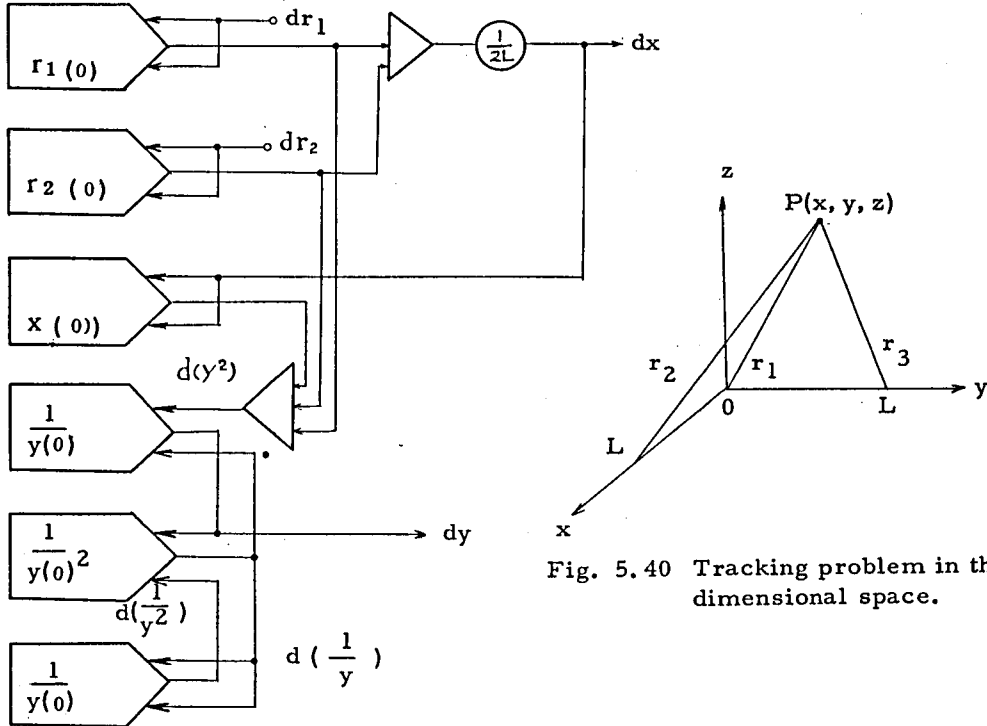


Fig. 5.39 DAC circuit for calculating  $x$  and  $y$  from  $r_1$  and  $r_2$  by eq. (5.162)

Fig. 5.40 Tracking problem in three dimensional space.

#### (v) Tracking in Three-Dimensional Space.

Referring Fig. 5.40 following relation holds.

$$\begin{aligned}
 r_1^2 &= x^2 + y^2 + z^2 \\
 r_2^2 &= (x-L)^2 + y^2 + z^2 \\
 r_3^2 &= x^2 + (y-L)^2 + z^2
 \end{aligned}
 \tag{5.164}$$

Rewriting the above equations leads to the following relation.

$$\begin{aligned}
 X &= \frac{1}{2L} (r_1^2 - r_2^2) \\
 Y &= \frac{1}{2L} (r_1^2 - r_3^2) \\
 Z^2 &= r_1^2 - X^2 - Y^2
 \end{aligned}
 \tag{5.165}$$

By successive differentiation we can derive  $dx$ ,  $dy$  and  $dz$  from  $dr_1$ ,  $dr_2$ , and  $dr_3$  in the following equations.

$$\left. \begin{aligned} dx &= \frac{1}{L} (r_1 dr_1 - r_2 dr_2) \\ dy &= \frac{1}{L} (r_1 dr_1 - r_3 dr_3) \\ d(Z^2) &= 2(r_1 dr_1 - x dx - y dy) \\ dZ &= \frac{1}{2Z} d(Z^2) \\ d\left(\frac{1}{Z}\right) &= -\left(\frac{1}{Z}\right)^2 dZ \\ d\left\{\left(\frac{1}{Z}\right)^2\right\} &= \frac{2}{Z} d\left(\frac{1}{Z}\right) \end{aligned} \right\} \quad (5.166)$$

These relations are represented by a computer circuit composed of eight integrators and three adders.

#### 5.7 Concluding Remark

An outstanding advantage of DAC is the simplicity of the control circuits. The individual computer elements operate by nothing other than the power supply, the clock pulse generator and the timing pulse generator. In this respect DAC is particularly suitable as a control computer for which the problems solved may be relatively limited. In the general purpose digital computer the machine capacity is of considerable scale whereas DAC can be built in any size depending on the calculation wanted to perform.

DAC has also a promising field of application where large scale analog computers are currently employed. The higher precision and higher computation speed of DAC will replace analog computers in those fields where financial problem is less important.

## Conclusion and Acknowledgement

The various ways of applying the analog computer to the problems of science and engineering which had been developed by the author were described in the foregoing chapters. Also described are the dynamic properties of analog computer elements. Specifying the dynamic property of a computer element is especially important in a certain problem where the system analyzed is less stable.

The new computer elements described in this thesis were developed by the author in order to use them for analyzing special problems which have been unable to be solved with usual computer elements.

In short this thesis treats various aspects of the analog computer technique which purposes solution of various problems by means of analog computer and the problems concerning the analog computer elements. Instead of rapid evolution of the analog computer as a hardware a deliberate preparation of the softwares has been left behind. The author's study on analog computers has always been carried out on the side of the software, that is, considering and analyzing physical system in terms of analog computer.

This is what we call analog computer technique. The results described in this thesis not only have been proved useful in actual analysis of the problems in the past several years in Tokyo-Shibaura Electric Co., Ltd. to which the author belongs, but also will be a valuable tool for solving many problems in the future.

The present author is grateful to the authors of the outstanding books 80) 81) 82) by which he was educated, to Prof. Chihiro Hayashi of Kyoto University for the continuous encouragement, to Prof. Bunji Kondo of Kyoto University for instructing and advising him in most of the problems treated in this thesis, and to Dr. Takeo Miura of Hitachi Co., Ltd. who has always been excellent adviser at the meetings of analog computer studies.

The sincere gratitude of the author are due to Mr. Sataro Aoki, the presi-

dent of Toshiba Engineering Co., Ltd, who assigned him the research work on the analog computer technique and gave him continuous advice and encouragement, to Dr. Shigenobu Wada, the deputy director of the Central Research Laboratory of Tokyo-Shibaura Electric Co., Ltd. who has led him in the course of research, and to Mr. Shozo Sotoyama who gave him continuous advice and encouragement. The author's gratitude are also due to Mr. Mituo Ito who has been an able assistant to the author.

Finally my heartiest thanks are given to the late Mr. Yasuhiko Saneyoshi who had given a large influence on the attitude of research of the author since <sup>he</sup>he joined to Tokyo-Shibaura Electric Co., Ltd, to whom this thesis is dedicated.

## REFERENCES

- 1) 守田, 実吉, 新井, 池田, 高橋「東芝低速相似型電子計算機 TOSAC II」東芝レビュー, 12, 8, 343, 1957
- 2) 守田, 新井, 高橋:「試作低速アナログ計算機について」電気連大, 186, 昭32-4
- 3) 新井, 鈴木, 高橋:「相似型電子計算機と工学問題の解析」東芝レビュー, 12, 953, 1957
- 4) H. Genchi, K. Aoki:「Interpretive Differential Equation Analyzer (IDEA) on U SSC」"Code for Reactor Computations" IAEA, 513, 1961
- 5) T. M. Stout:「A Block diagram approach to Network Analysis」Trans. AIEE, 71, II, 225, 1952
- 6) 高橋, 伊藤:「アナログ計算機による電気回路解析法」電気東京支部大会, 56, 1957-11
- 7) 平山:「アナログ計算機の位相幾何学的プログラミング」信学会 回路網理論専門委, 昭33-2-7
- 8) 高橋:「微分解析機による回路網シミュレーション」電気連大, 25, 昭和36-4
- 9) 高橋:「微分解析機による回路網シミュレーション」電学誌 81, 878, 1852 昭和36-11
- 10) Y. Takahashi:「Theory of the Simulation of Network on the Differential Analyzer」Proc. 3rd International Analog Computation Meetings, 496, 1962
- 11) 近藤, 小野寺「回路のトポロジー」岩波現代 応用数学講座, P10, 昭-34
- 12) 近藤, 小野寺「回路のトポロジー」岩波現代 応用数学講座, P11, 昭-34
- 13) R. Onodera:「Topological Synthesis of Transfer Admittance Matrices」IRE Trans, CT-7, 2, 112 1960-6
- 14) 岡田:「現代数学による回路網理論(その2)」電学誌 72, 551 昭-27
- 15) G. W. Smith, R. C. Wood:「Principle of Analog Computation」Mc Graw-Hill, 24, 1959
- 16) 特許第293913号(昭和37-2-12)  
高橋, 伊藤:「分圧器装置」特許公報 昭36-14864
- 17) 高橋:「アナログ計算機用遅延装置の「良さ」について」電気連大, 203, 昭34-4
- 18) 高橋:「遅延装置の「良さ」の基準」アナログ計算機研究会資料, 昭34-5-12
- 19) L. C. Tohnson:「Analog Computer Technipues」Mc Graw-Hill, P129, 1956
- 20) G. S. Stubb, C. H. Single:「Transport Delay Simulation Circuits」AEC Report, WAPD-T-38 & Suppl. 1954
- 21) E. G. Holzmaun:「Variable Transport Lag Simulation」Nuclear Eng. & Sci. Conf. 112, 1958
- 22) 林, 近藤:「遅延素子を用いた電子管式サージアナライザの試作」電気関西支部大会, 94, 昭31-10
- 23) R. S. Stone, R. A. Dandl:「A Variable Function Delay for Analog Computer」IRE Trans, EC-6, 187, 1956-9
- 24) J. M. Janssen:「Discontinuous Low Frequency Delay Line with Continuously Variable Delay」Nature 169, 148 1952
- 25) L. Ensing:「Delay Line Synthesizer Process Simulator」Proc. 2nd International Analog Computation Meetings, 504, 1956
- 26) 三浦他:「むだ時間要素の試作と応用」電気連大 236 昭33-5
- 27) J. Wood:「Controlling the Pure-Delay Plant」Instr & Automation, 30, 9, 1720 1957



- 28) D. C. Reukauf:「Simulate Transport Lags with Magnetic Tape」Control Eng. 4, 6, 146 1957
- 29) 高井他:「相似計算機用むぞ時間要素の試作」電気東京支部大会, 45, 昭32-11
- 30) 高橋, 伊藤:「アナログ計算機用可変時間遅延装置」電気東京支部大会, 89, 昭34-11
- 31) 高橋, 伊藤:「アナログ計算機の自動試験装置」電気連大, 409, 昭35-7
- 32) 高橋:「アナログ計算機の演算試験法」エレクトロニクスダイジェスト, vol26, 154, 1961
- 33) 高橋, 伊藤:「アナログ計算機の自動試験装置」東芝レビュー, 15, 9, 1030, 1960
- 34) H. E. Harris:「New Techniques for Analog Computer」Instr & Automation 30, 5, 894 1957
- 35) Reeves Instrument Co:「Efficient Utilization of Analog Computer」March, 1957
- 36) Editor:「The Simulation Council News Letter」Instr. & Automation, 311, 1848 1958
- 37) R. P. Sykes:「A Preventive Maintenance Program for Large General Purpose Electronic Analog Computers」IRE Conv Record, 6, Pt. 4, 191 1958
- 38) 高橋, 伊藤:「アナログ計算機の自動試験装置」特許公報 昭34-62293
- 39) 沼倉他:「サーボ掛算器の研究(第2報)」電気連大 239, 昭33-4
- 40) J. G. Truxal:「Control Engineers Handbook」P, 13-6, 1958
- 41) 高橋:「AC サーボ系の伝達関数」自動制御5, 4, 121, 昭-33
- 42) 高橋:「ACサーボ系の伝達関数について」  
第98回自動制御研究集会, 資料P. 1 昭33-3-4
- 43) 高橋, 「交流サーボ系の伝達関数の一形式」電気連大 189 昭33-5
- 44) H. Chestnut, R. W. Mayer:「Servomechanisms and Regulating System Design」vol. II, P. 187 John Wiley & Sons, Inc. 1955
- 45) D. Morris:「A Theoretical and Experimental Method of Modulation Analysis for the Design of AC Servo Systems.」"Automatic and Manual Control" by A. Tustin, P. 521 London, 1951
- 46) 沼倉他:「サーボ掛算器の解析」電学誌 77, 826, 1009 昭32-8
- 47) H. E. Blanton:「Carrier Compensation for Servomechanisms」Journ. Franklin Institute. 246, pp391~407, pp, 525~542 1950
- 48) 高橋:「チョッパ式変調回路の伝達関数」電学誌 79, 846, 291 昭34-4
- 49) 高橋:「チョッパ回路の伝達関数の研究」信学会, 回路網理論専門委, 昭33-12,
- 50) 高橋, 若林:「チョッパ回路の伝達関数の計算法」電気連大 186, 昭33-5
- 51) 加藤, 池上, 井上:「断続型増巾器, 入力回路の周波数特性について」電気関西支部大会, 619 昭29-11
- 52) F. H. Kranz, O. M. Salati, R. S. Berkowitz:「A Study of the Transfer Function of Contact-Modulated Amplifiers」Trans AIEE. App & Industry No. 29, 23, 1957-3
- 53) 当麻, 栗屋:「チョッパ回路の伝達関数」電学誌78, 837, 683, 昭33-6
- 54) 沼倉, 阿部, 衣川:「チョッパ回路の伝達関数」電学誌, 79, 845, 187 昭34-2
- 55) 岡崎:「断続式電位計の動作解析」島津評論10, 2, 78, 昭29
- 56) 沼倉:「チョッパ回路の周波数特性と伝達関数」アナログ計算機研究論文集, p232, 昭33
- 57) 当麻:「チョッパ回路の解析」信学会回路網理論専門委, 昭33-12-9
- 58) 沼倉, 阿部:「チョッパ回路の伝達関係」信学会回路網理論専門委, 昭和33-12-9

- 59) 中津山：「Fマトリクスよりチョッパ回路の伝達関数を求める計算法」電気連大，140 昭34-4
- 60) 高橋：「アナログ計算機による電気回路解析法」アナログ計算機研究会論文集。P36 昭-33
- 61) 山下編：「電子計算機，アナログ計算機編」P. 311 (執筆高橋) 昭-34
- 62) H. M. James, N. B. Nichols, N. S. Phillips：「Theory of Servomechanisms」McGraw-Hill 1947
- 63) 山下編：「電子計算機，アナログ計算機編」P. 337 (執筆高橋) 昭-34
- 64) 高橋：「オートマテック プログラミングの一例(境界値問題)」アナログ計算機研究会資料 昭33-12-10
- 65) 高橋：「アナログ計算機による境界値問題の解法」電気東京支部大会 56, 昭33-10
- 66) 特許第298273号  
高橋「計算装置」特許公報 昭36-22055
- 67) 菅野：「電子管式アナログ計算機による境界値問題の一解法」電学誌 76, 812, 493 昭31-5
- 68) L. C. Johnson：「Analog Computer Techniques」Mc Graw-Hill, P. 203  
1956
- 69) 特許出願 昭38-5895号
- 70) 萩原：「遅延帰還による周期信号の検出」電気連大 745 昭31-4
- 71) 高橋，玄地，高松：「DAC 数字式アナログ計算機」電気連大 423 昭35-7
- 72) 高橋，玄地：「数学式アナログ計算機の原理」アナログ計算機研究会資料，昭和35-9-12
- 73) 高橋，玄地，中野：「数字式アナログ計算機とその応用」計測と制御 1, 4, 285, 昭-37
- 74) 高橋，玄地，中野：「数字式アナログ計算機 DAC-I」東芝レビュー 17, 7, 735 昭37-7
- 75) 高橋，玄地：「数字式アナログ計算機DAC, その応用」第3回自動制御連合講演会，285, 昭-35
- 76) R. E. Sprague：「Fundamental Concepts of the Digital Differential Analyzer Method of Computation」MTAC 6, 37, 41, 1952
- 77) J. F. Donnan：「The Serial-Memory Digital Differential Analyzer」MATC 6, 37, 102, 1952
- 78) M. Palvesky：「The Design of the Bendix Digital Differential Analyzer」Proc. IRE, 41, 10, 1352 1953
- 79) R. C. Hansen, L. L. Bailin R. W. Rutishauser：「On Computing Radiation Integrals」Commun. of ACM, 2, 2, 28, 1959
- 80) G. A. Korn, T. M. Korn：「Electronic Analog Computers」Mc Graw Hill 1956
- 81) F. H. Raymond：「Le Calcul Analogique et Machines Electroniques」Revue d'Optique, Paris 1954
- 82) W. W. Soroka：「Analog Methods in Computation and Simulation」McGraw Hill, 1954
- 83) 萩原：「相関函数測定法における遅延時間の揺ぎと雑音中の周期信号の検出」NHK技術研究 26, 1, 昭31-7
- 84) 関：「遅延帰還の理論と応用」信学誌 39, 1, 9 昭31-1